SWITCHED-CAPACITOR FILTERS AND THEIR APPLICATION IN DATA COMMUNICATIONS

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I hereby declare that the contents of this thesis are based on my own research.

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ABSTRACT

There have been considerable developments in the field of switched-capacitor filter design over the past decade. Those developments which allow the operating frequency range of switched-capacitor filters to be extended are considered.

The solution to the approximation and synthesis problems for l.d.i.-based switched-capacitor ladder filters discovered by Scanlan is explained. Computer software which implements his technique for low-pass filters is presented. A number of techniques for synthesising the network are investigated. It is shown that numerical difficulties limit the order of filter which can be synthesised. The sensitivity properties of switched-capacitor ladder filters are explored. A technique, which has been implemented in software, for evaluating the amplitude sensitivity of such filters is described. This program is used to demonstrate that the frequency variable terminations in the equivalent circuit of the switched-capacitor ladder filter adversely affect its sensitivity properties.

Circuit topologies which result in improved high frequency performance are considered, and a fully differential filter structure for high frequency operation is proposed. Circuits are presented for a digitally programmable switched-capacitor line equaliser and optimisation techniques for its design are investigated. The extension of the design to incorporate adaptive operation is discussed, and circuits based on the above designs which have been fabricated at the National Micro-electronics Research Centre (N.M.R.C.) in Cork are described.

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CONTENTS

Considering first the eighth-order filter, the expected passband response, as determined using (3.35), is shown in Fig. 3.11. The plot obtained is based on the response calculated at sixty four evenly spaced frequencies in the passband. The response obtained at each point is marked by a cross in Fig. 3.11, and the plotting routine joins the points by straight lines to approximate a continuous curve. The points plotted are, to a very high accuracy, in the positions expected from (3.16), indicating that $S_{11}(\lambda)$ has been obtained correctly. (The apparent droop in the passband response around $f/f_S = 0.06$ occurs because only a few points are plotted there - there are numerical difficulties associated with calculating (3.35) at closer frequency intervals in this region.)

Table 3.5 shows the element values obtained for the equivalent circuit of Fig. 3.9(a) for the three synthesis methods considered. The pass-band response obtained by simulating the three filters in Table 3.5 are shown in Figs. 3.12, 3.13 and 3.14 for the first, second and third methods. Clearly the passband responses for the first and second methods are not equiripple, that in Fig. 3.12 deviating most from that intended (i.e. Fig. 3.11). In contrast, the correspondence between Figs. 3.11 and 3.14 is excellent.

The corresponding element values for a ninth-order filter are shown in Table 3.6. Again, $S_{11}(\lambda)$ has been obtained accurately, as demonstrated by Fig. 3.15. The value of the last inductor for the first two methods is negative, indicating that these methods have failed to synthesise the filter correctly. In fact, the element values for the second method result in an unstable filter, so no plot of passband response can be obtained. The time domain simulation of the filter synthesised using the second method, when transformed into the frequency domain using the FFT, results in the pass-band response of Fig. 3.16. The test of [87] shows this to be an unstable filter. Once again, the results obtained by the third method are excellent, as shown in Fig. 3.17.

The superiority of the method of [87] is thus demonstrated. Using the values obtained by this method as a reference, it can be seen that, for the other two methods, the values of the extracted elements diverge appreciably from the correct values after five elements have been extracted. Improvements in the numerical techniques used might improve this figure (e.g. both methods return an incorrect value for the load termination, which can be calculated before commencing the synthesis as $Z_{in}(\lambda=0)$, and this error might be corrected for).

Chapter One: INTRODUCTION

The field of switched-capacitor filters has attracted considerable attention over the past decade. This interest stems from the suitability of such filters for integration using the MOS processes which have been developed for the integration of increasingly sophisticated digital circuitry. Recent developments in switched-capacitor filter technology and in the theory of operation of such circuits allows their usable frequency range to be extended beyond the voice-band. This work investigates some of these developments, and their application in the field of digital data communications. The topics discussed will now be briefly outlined.

Chapter Two:

The basic concepts of switched-capacitor filters are introduced. There follows a discussion of developments in the field concentrating on those areas of most relevance to subsequent chapters. Techniques which have been developed for the analysis of switched- capacitor filters are listed. Synthesis techniques are then discussed, in particular those which have been developed for the so-called switched-capacitor ladder filters. Circuit techniques for overcoming the limitations of practically implemented filters are briefly considered. The chapter concludes by mentioning some practical applications of switched- capacitor filters, focussing on applications in telecommunications.

Chapter Three:

Exact design techniques for the class of switched- capacitor filters usually referred to as l.d.i. ladder filters are considered, concentrating on the low-pass case. These filters are derived from the signal flowgraph of passive ladder prototypes. Exact design techniques are a pre-requisite for high-frequency operation of these filters. The original stray-sensitive designs for switched- capacitor ladder filters are briefly described. The stray-insensitive integrators used in modern filter designs are presented, and clock phasing schemes which result in their implementing lossless discrete integration when incorporated in ladder filter topologies are discussed. The exact design procedure introduced by Scanlan for this class of filter is outlined. The algorithms used in implementing the design procedure on computer are described. Various techniques which have been proposed for the synthesis of these filters, given the input impedance as calculated using the

method of Scanlan, are presented, along with details of their computer implementation. Alternative design techniques introduced by other authors are briefly discussed. Results obtained from sample runs of the synthesis program are presented for various algorithms, and the chapter concludes with a brief discussion of the numerical difficulties associated with the design technique.

Chapter Four:

The concept of sensitivity is introduced, and the argument propounded by Orchard explaining the low passband sensitivities of doubly-terminated reactance two-ports is presented. A number of techniques for the evaluation of filter sensitivities are described. A formula for calculating the sensitivity of the squared amplitude to element value variations for switched- capacitor ladder filters is developed. The reasons for expecting the passband sensitivity of a switched-capacitor ladder filter to be inferior to that of a passive LC ladder filter designed to the same specifications are explained. A filter response which is expected to feature minimal passband sensitivity is proposed. This is not an approximation to the ideal low-pass response, but is instead intended to demonstate the sensitivity properties of switched- capacitor ladder filters. The passband sensitivities, as calculated by computer, for high-order switched- capacitor ladder filters are presented, as a practical example of sensitivity evluation.

Chapter Five:

Topologies which limit the high frequency performance of switched-capacitor filters are discussed. Circuit techniques which result in improved filter response at high frequencies are investigated. The transfer functions for fully differential switched- capacitor integrators are derived. The advantages of such circuits for high frequency operation are described. A list of requirements for a filter structure for high frequency operation is presented. The limitations which are consequently imposed on filter topology are explored. In particular, it is shown that a filter with a second order (z-plane) numerator (as do standard biquad structures) requiresthree op-amps and thus can possess a third-order denominator. A single-ended filter satisfying the above constraints is presented, and an expression for its transfer function is obtained. Hence a fully-differential filter structure is found. It is shown that this structure can incorporate a cosine-filtering action, and that, by means of a simple topological transformation, any z-domain transfer function with two zeros and three poles can be implemented. Finally, an algorithm

is presented for obtaining capacitor values for the new filter structure.

Chapter Six:

The options available for bidirectional baseband digital communications are briefly discussed. The potential of switched- capacitor filters for application in this area is assessed. The components required of a switched- capacitor line equaliser are listed. Circuitry for the implementation of such an equaliser is presented. Design techniques for the filter sections are introduced, and the resulting element values are tabulated. Optimisation techniques for the equaliser design are presented, for use in both the time domain and the frequency domain, and practical details of their implementation are discussed. The results obtained from the optimisation process are presented, and the limitations of the methods used are discussed. The extension of the equaliser design to incorporate adaptive operation is investigated. Previous techniques used to achieve this are explored, and circuitry is proposed to perform the adaptation. Finally, details are presented of some filter sections which have been integrated at the National Micro-electronics Research Centre to test the equaliser design.

The broad conclusions to be drawn from the work presented above are listed in Chapter Seven, as well as some suggestions for further research.

Chapter Two: SWITCHED CAPACITOR FILTERS - A REVIEW

2.1 Basic Concepts.

The concept of using switches and capacitors to effect frequency selective electrical networks is of comparatively recent origin. Fettweis, in a review of early work [1] points out that the term switched- capacitor filter was used (in [2]) as early as 1971, and the concept had been mooted in an English-language journal in 1972 [3] by Fried. However, it was not until 1977 [4,5] that the significance of the concept was widely appreciated, in that it made the integration of precise analog filters using a standard MOS process feasible.

Analog filters had proved difficult to integrate using conventional means. Filters using inductors were obviously impossible to integrate. RC-active filters, however, although they could be integrated, presented two major problems. The absolute value of integrated resistors and capacitors cannot be precisely controlled, and hence the filter parameters, which are dependent on RC products, are imprecise. Resistors of high value and acceptable linearity, of the type typically required for RC-active filters, require large die areas [6].

An alternative technique for monolithic analog filtering is to use transversal filters based on the CCD principle [7]. However, the superiority of the switched- capacitor technique for most applications was readily apparent [8]. In recent years, new techniques for monolithic analog filtering have been developed which, unlike the above techniques, operate in continuous time. However, this has not led to any decline in the popularity of switched- capacitor filtering as a research topic, as demonstrated, for example, by the number of sessions held on the subject at the International Symposium for Circuits and Systems at Helsinki in June '88.

The earliest switched- capacitor filters were based on replacing the resistors in a conventional active-RC design by nominally equivalent switched-capacitors [4]. The equivalence is only valid for signal frequencies much lower than the sampling rate, in which case the filter can be approximately regarded as operating in continuous time. A switched- capacitor equivalent of the conventional

active-RC integrator proved to be a versatile building block for switched- capacitor filters [5] but suffered from stray- sensitivity. This means that the stray capacitances which are inevitably present between each capacitor plate and the substrate in an integrated filter affect the transfer of charge through the filter. However, *stray- insensitive* circuits for performing the same operation have been developed [5,9] for both inverting and non-inverting integration, and have become standard elements of switched- capacitor filters. These filter sections are shown in Fig. 2.1.

It was recognised that, when these integrators were analysed rigorously as sampled-data systems, the difference equations describing their operation corresponded to the *linear discrete integrator* (l.d.i.) [10], first proposed by Bruton as a numerical approximation to integration for use in digital filters, and the *damped discrete integrator* (d.d.i.), which performs the l.d.i. operation with the addition of negative feedback from the output to the input. Hence these terms are often used to refer to the integrator circuits shown.

Other first order sections have been proposed, such as those in [11], which realise integrators based upon the bilinear transform. Many of these building blocks are stray- sensitive, although stray- insensitive equivalents can often be found [12-14]. There are also quite different techniques of performing switched-capacitor filtering, such as using voltage inverting switches [15,16], or other techniques of simulating wave digital filters [e.g. 17]. However none of the rival techniques currently feature the combination of simple circuitry and stray-insensitive operation provided by the circuits of Fig. 2.1, which are the compelling reasons for their adoption as the basis of most integrated systems featuring switched- capacitor filtering [18].

The difference equations describing the operation of the d.d.i. circuits of Fig. 2.1 are

$$V_O(n) = C_2/(C_2+C_3)\ V_O(n-1) + C_1/(C_2+C_3)\ V_1(n-\tfrac{1}{2})$$

and

$$V_O(n) = C_2/(C_2+C_3)\ V_O(n-1) - C_1/(C_2+C_3)\ V_1(n)$$

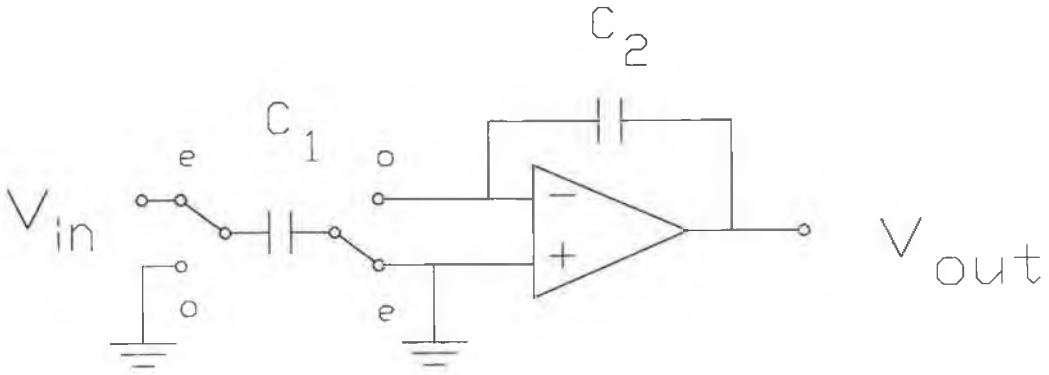


Fig. 2.1(a) : non-inverting l.d.i.

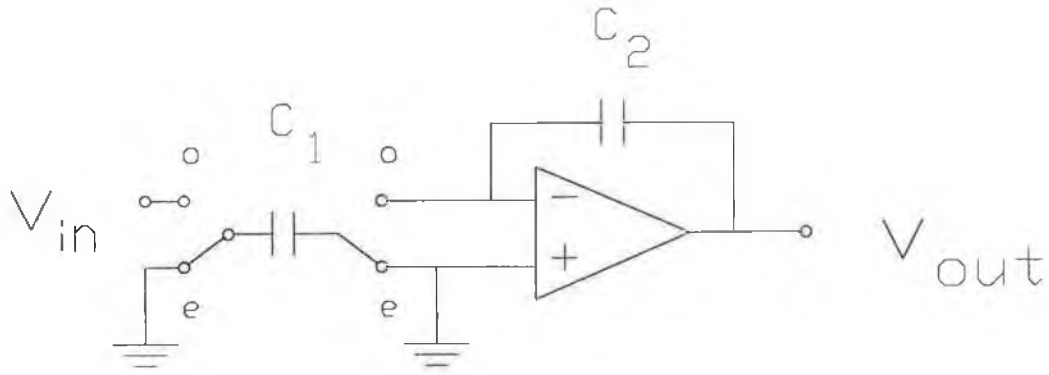


Fig 2.1(b) : inverting l.d.i.

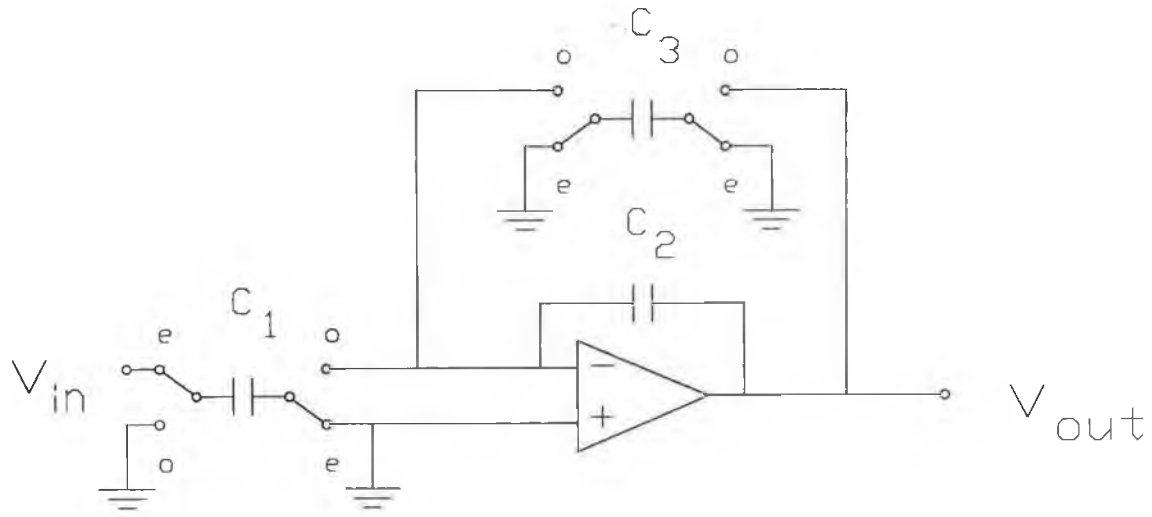


Fig. 2.1(c): Non-inverting d.d.i.

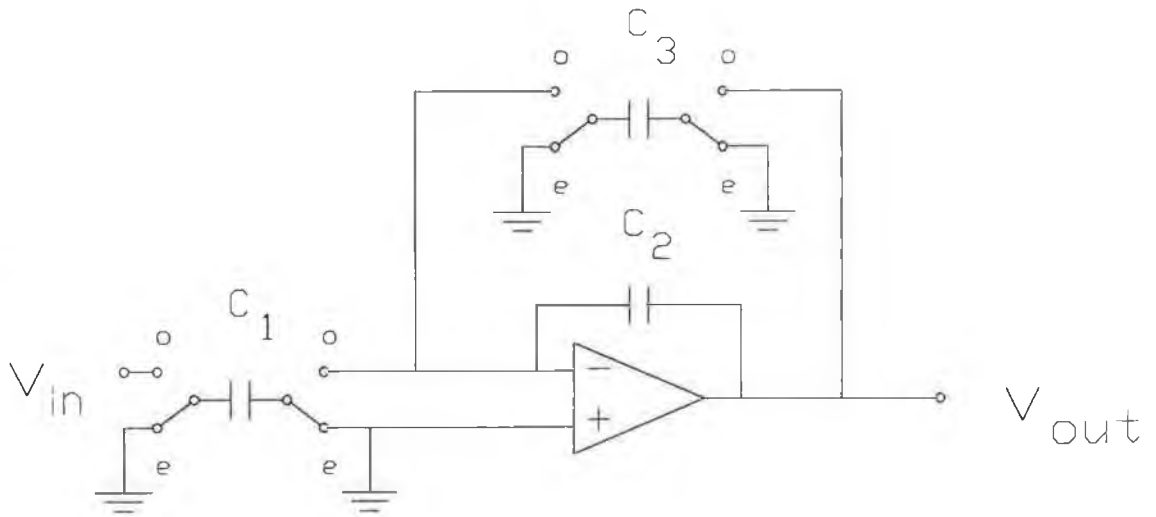


Fig. 2.1(d): inverting d.d.i.

By the addition of an unswitched capacitor from the virtual earth terminal to a second input V_2, a simple gain term is added to the expression for the output. Coupling two integrators, one inverting and the other non-inverting, and thereby providing negative feedback, results in a biquadratic transfer function in the z-domain. A number of structures for such biquads have been proposed [9,19-23] of which that in [23] (which is reproduced in Fig. 2.2) has been particularly popular. The design considerations for these biquad structures have been further investigated in [24-26] and Bermudez has presented an optimisation approach which selects the most appropriate from the wide range of possible biquads for a particular application [27]. Huang and Sansen have suggested the use of a 'split integrating capacitor' to reduce the capacitance ratio spread in biquads [28].

High order filters can readily be synthesised using cascaded biquads [21]. However, for low sensitivity, a design based on the simulation of a doubly terminated passive lossless ladder should be used. Orchard demonstrated [29] that such passive filters, when designed so that maximum power transfer is achieved at some frequencies in the passband, can be expected to feature low sensitivity in the passband, by appealing to simple arguments of power transfer. It follows that any active filter based on the simulation of such passive prototypes should feature low sensitivity in the passband. Since ladder filters also feature low stopband sensitivity (all circuit elements contribute to the stopband loss) such filters are usually chosen as the prototype for the active filter design.

In the case of switched- capacitor filters, simulations based upon the 'leapfrog ladder' or signal flowgraph technique for simulating passive LC ladder filters have proved most effective, since they can be implemented with the stray-insensitive circuits of Fig. 2.1 [30,31].

2.2 Analysis Techniques.

As the complexity of switched- capacitor circuits continued to increase, a need for advanced techniques for the analysis of such circuits arose. A variety of methods has been proposed for performing such an analysis. These range from techniques for manually determining a switched- capacitor filter transfer function by inspection or hand calculation [32-38] to techniques rigorously developed from

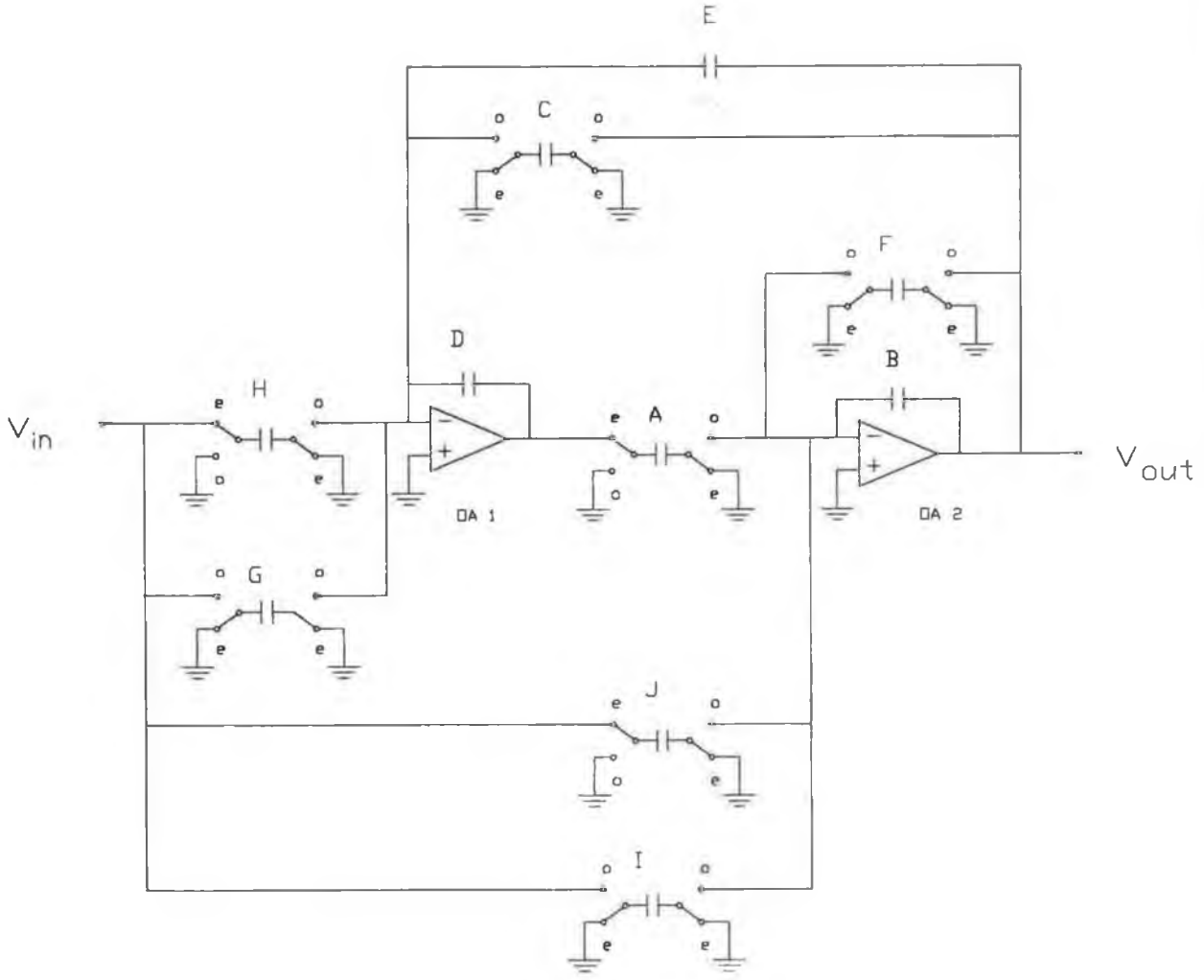


Fig. 2.2: Fleischer-Laker Biquad

circuit theory [39-44] which allow computer-aided analysis or simulation of complex circuits [e.g. 45,46]. These techniques are based on a few fundamental approaches to the analysis problem [47]. These include the charge formulation approach, based on the principle of conservation of charge [34,48], the use of nodal analysis [49] and modified nodal analysis [44], and on the use of the indefinite admittance matrix [41]. Another approach is to use equivalent circuits where, for example, two-phase switched- capacitor elements or subcircuits are replaced by equivalent four-port networks [40,50].

A number of computer programs have been written to analyse switched-capacitor networks using these techniques, such as those listed in [51]. Most of these programs assume ideal circuit elements - for example SWITCAP [52,53] assumes the network consists only of ideal capacitors switches and voltage sources. Resistors can be simulated approximately by using the resistor-switched capacitor equivalence of [4] and a high sampling rate. More rigorous analysis of resistive switched- capacitor circuits requires the solution of differential difference equations [47]. Solutions to this problem were formulated specifically for the analysis of switched- capacitor networks in [54,55]. Other solutions to this problem have recently been proposed [56-58]. The latter approach allows matrix expressions for the frequency response of a general linear resistive switched- capacitor network to be obtained. Thus recently available analysis programs, for example the NISCAP program used in [59], and SWAP (marketed by Silvar-Lisco Inc.) can accurately analyse such effects as the finite bandwidth of real op-amps and non-zero on-resistance of switches.

As the performance of switched- capacitor filters has increased, further specialised analysis tools for investigating non-ideal operation have been developed. The effect of finite gain-bandwidth on switched- capacitor filters has been analytically investigated [60-62] and analysis procedures which allow for op-amps, in an otherwise ideal switched- capacitor network, which have finite gain and bandwidth have been developed [63,64]. Other more subtle non-idealities of switched- capacitor networks have been investigated, such as errors in charge transfer [65], the effects of the resulting residual charge [66], and the transient response of practical switched- capacitor networks [67]. Such non-idealities give rise to frequency domain distortion, which is analysed in [68]. These non-ideal factors limit the performance of switched- capacitor filters as the clock rate is increased, and such frequency limitations are discussed in [69]. Another major difficulty with practical switched- capacitor filters has been the noise generated [6] and this has

been analysed in [70-73].

2.3 Synthesis Techniques.

Advances in the analysis of switched- capacitor filters have been matched by developments in the area of circuit synthesis. The earliest synthesis techniques were simply those already available for active filters, but which are only approximately valid for switched- capacitor filters [30]. The resulting switched-capacitor filter reproduces the response of the corresponding active-RC filter only for signal frequencies much less than the filter sampling rate. Accurate techniques must account for the sampled-data nature of the filters. This can readily be done for filter designs based on cascaded biquads [20]. For example, the discrete-time transfer function to be implemented can be derived from a continuous-time function obtained using traditional methods, via a suitable transformation, typically the bilinear transformation [74]. The z-domain poles and zeros are then allocated to the biquad sections (using, for example, the technique of [75]). Each biquad is then synthesised by matching co-efficients with its discrete-time transfer function and scaling for maximum dynamic range [23]. No major innovations are required in this design procedure which parallels existing techniques for the synthesis of cascaded biquads.

The exact synthesis of switched- capacitor filters based on the simulation of doubly-terminated passive LC ladders represented a new problem in circuit theory. One of the simplest such filters is the all-pole lowpass ladder. The difficulty in synthesis arises because the variable used to simulate integration in filters based on the circuits in Fig. 2.1 is the variable $1/\gamma$ where

$$\gamma = \sinh(sT/2) = \tfrac{1}{2}(z^{1/2} - z^{-1/2})$$

and where T is the filter clock period, $1/s$ is the Laplace Transform of the integration operator, and $z^{-1} = e^{-sT}$ is the Laplace Transform of the delay operator, for a delay of T [10,76]. If a filter is realised which implements the signal flowgraph of an all-pole ladder exactly but with the variable s replaced by γ, it will be unconditionally unstable. This is because, if the filter has a z-domain pole at $z_1 = e^{-s_1 T}$, it will also have a pole at $z_2 = -z_1^{-1}$, since the value of γ is same at $z = z_1$ and $z = z_2$. Thus it is impossible for all the poles to be inside the unit circle in the z-plane, or to be on the right hand side of the

s-plane, as is required for a stable filter. Stable filters can be realised by modifying the filter operation so that it is not described simply by a function of γ. In fact the terminations of the γ-mapped filter corresponding to the all-pole ladder cannot be realised using the circuits of Fig. 2.1 [77,78]. Consequently, terminations realisable using the damped discrete integrator of Fig. 2.1 are employed, resulting in an equivalent circuit, in ladder form, of the type shown in Fig. 2.3.

The approximate design technique first employed [31] ignored the frequency variation of the terminations in Fig. 2.3, thereby allowing the classical results for the synthesis of LC ladder circuits to be applied. Consequently the frequency response obtained matched the designed-for response only for frequencies f where $2\pi fT << 1$, in which situation the approximation $Rz^{-1/2} \simeq R$ is valid. In practice, this means that the filter sampling rate must be much greater than the filter cutoff frequency if the filter is to operate satisfactorily.

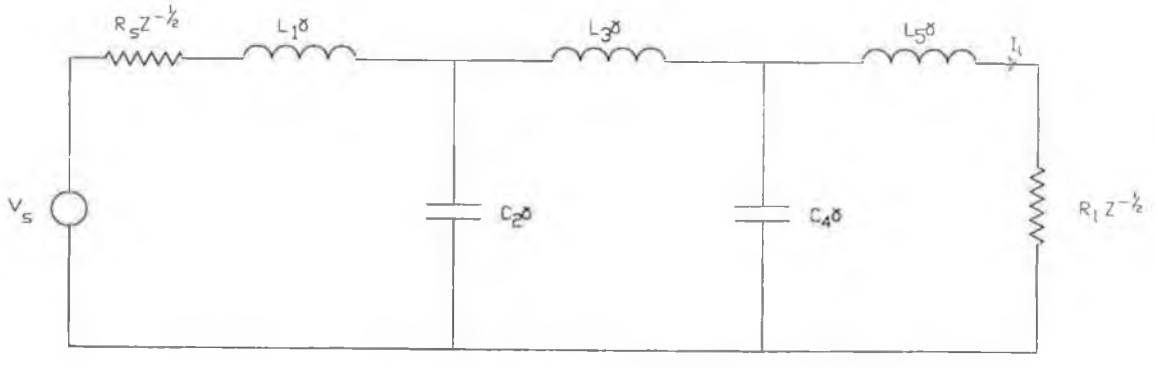


Fig. 2.3: Equivalent Circuit of Fifth Order l.d.i. based low pass filter.

A new synthesis technique was required for the accurate synthesis of signal-flowgraph based switched- capacitor ladder filters, which simulate networks of the type shown in Fig. 2.3. Lee and Chang bypassed this problem by performing a topological modification on the prototype filter which allowed the bilinear transform instead of the l.d.i. transform to be used in the synthesis [79]. The resulting filter contains unswitched capacitors connected in a manner used, in approximate techniques, to introduce transmission zeros, such as are required in elliptic filters [31]. Hokenek and Moschytz used a similar technique, using the bilinear transform to derive a filter structure, which, following admittance scaling, could be realised using circuits similar to those of Fig. 2.1. (together with unswitched capacitors) but with clock phases such that integration of the l.d.i. type was not performed [80]. Another suggestion, by Choi and Broderson [78], was to change the damped discrete integrators which simulate the ladder terminations so as to simulate conjugate terminations. This reduced, but did not eliminate, the high frequency error. Davis and Trick used what might be termed a 'brute force' method to perform the synthesis, which required the solution of a set of nonlinear equations [81]. This technique obviously becomes unwieldy for filter orders higher than three.

An exact solution to the synthesis problem for this class of filter was presented by Scanlan [76]. The power of the technique proposed by Scanlan stems from the equivalence established between switched- capacitor filters based upon the l.d.i. variable, and a class of distributed- parameter filters. This allows approximation and synthesis techniques for switched- capacitor filters to be developed by analogy with the existing wealth of techniques available for the design of filters employing unit elements [82,83].

In fact, an exact synthesis procedure for l.d.i.- based low pass filters had already been published as early as 1977 [84] by Vaughan-Pope and Bruton. Their paper, however, does not provide a general solution to the approximation problem for this class of filters. Also, their method, which involves the use of mirror-image and antimirror-image z-domain polynomials, does not relate the synthesis problem for the l.d.i.- based filter to that for a classical filter type, as that of Scanlan elegantly does. This solution to the synthesis problem does not appear to have come to the attention of the switched- capacitor filter research community until its relevance was described by Yassine [85], and was not extended to high pass filters until 1984 [86].

The range of application of the circuits of Fig. 2.1 was soon extended to include other filter types. Transmission zeros could be easily added to a low pass filter by adding unswitched capacitors to provide simple gain terms, as shown in [31]. By substituting two- integrator loops (to form simple biquads) for the integrators of the low pass filter, bandpass filters could be designed [77].

The technique of [76] was soon developed to encompass these filter types. In [87] Baher and Scanlan presented a simple test for the stability of the l.d.i.- based low pass ladder which follows directly from the work of [76] (a more complicated test is given in [88]) and a new synthesis algorithm based on the derivation of the transmission matrix for the ladder. Taylor [89] showed that the method could be applied to the synthesis of low pass filters with finite transmission zeros by considering the example of a third order elliptic filter. Tawfik *et al.* [90] extended the technique to bandpass designs using a lowpass to bandpass transformation, and presented an equation for the required form of the transducer power gain for a bandpass l.d.i. ladder-based switched- capacitor filter obtained by replacing each inductor or capacitor by a series or parallel resonant LC section. A more powerful solution to this problem was presented by Baher and Scanlan [91]. Their technique did not require the passband to feature geometric symmetry.

Datar and Sedra also published their method for the exact synthesis of switched- capacitor ladder filters [92]. Lowpass filters with and without transmission zeros were considered in detail and a fourth order bandpass example was given. The method used was essentially equivalent to that proposed by Scanlan, with the exception that a second switched capacitor had been added to the input stage of the switched- capacitor ladder, as shown in Fig. 2.4, which resulted in a factor $\frac{1}{2}(1+z^{-1})$ appearing in the filter transfer function. Thus the approximation problem differed slightly from that considered by Scanlan. Subsequently Datar and Sedra extended their results to the highpass case [93]. Previous exact synthesis methods based on bandpass ladder simulation had used the bilinear transform [94] or a variant thereon [80,95]. Baher also extended the method of [76,87] to the highpass case [96], allowing the number of transmission zeros at the origin to be specified.

The approximations used for the various ladder structures have been summarised by Baher in [97]. All of these approximations were amplitude approximations only, but were extended to cover linear phase responses in [98,99].

An alternative approach to the design of linear phase switched- capacitor filters was presented by Lish [100].

Other authors presented variations on the theme introduced by Scanlan. Yassine [85] presented a method similar to Scanlan's, but which was claimed to offer the advantage over the earlier method of not being limited to the use of the l.d.i. transformation from continuous time to discrete time. His method does not include a solution of the approximation problem. Instead, a continuous-time transfer function is selected, and converted into discrete-time using any suitable transformation [101]. The characteristic function is then obtained in a manner equivalent to that proposed by Scanlan, and the method of [87] for finding the transmission matrix parameters of the filter is applied. Another approach to l.d.i. based design has been that of Taylor and Mavor for the case of highpass and lowpass filters. Their technique reduces the signal flowgraph of a cascade of unit elements to a form suitable for implementation using damped differential integrator circuits, so that no new synthesis technique is required [102-104].

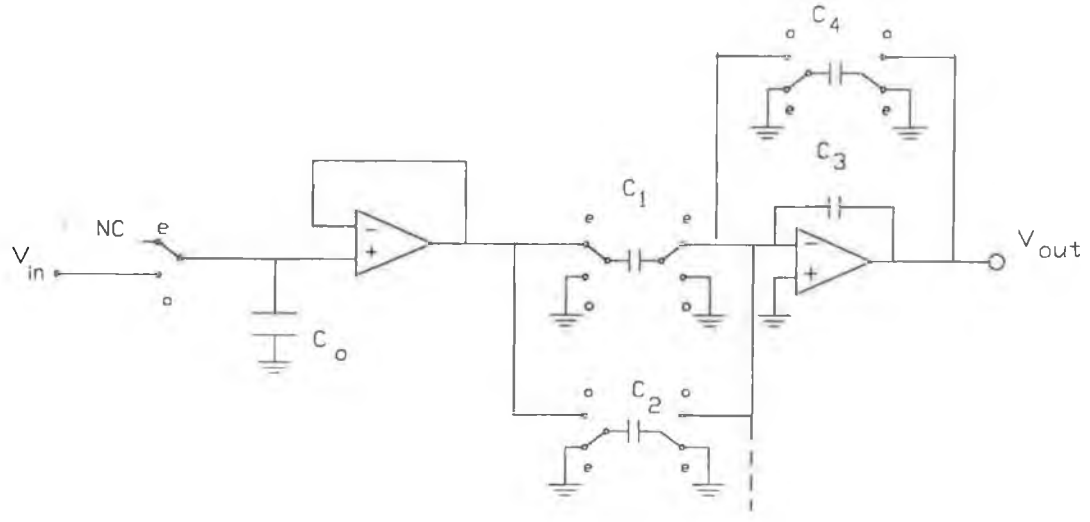


Fig 2.4: Feed-in branch realising transmittance of form $(1+z^{-1})$

The maturity of this area of switched- capacitor filter investigation in only a few years is indicated by the existence of CAD software which incorporates the Scanlan/Baher technique [105].

For complex prototype filters, many choices of state variable or signal flowgraph representation are possible, making the 'leapfrog' simulation technique more difficult to apply. To avoid this difficulty, new techniques can be used for deriving the switched- capacitor filter from the passive prototype, such as the use of intermediate transfer functions [106] or LU decomposition [107].

2.4 Technological Considerations for SC Filters.

As experience has been gained in the practical realisation of switched-capacitor filters on MOS integrated circuits, new techniques have been proposed for overcoming difficulties in their implementation. Hasler [108] has stated conditions for a switched- capacitor network to be stray-insensitive, and has presented an algorithm for obtaining a stray-insensitve implementation from one that is sensitive to stray capacitance [109]. Numerous authors have proposed techniques for the reduction of the effect of finite op-amp gain on the performance of switched-capacitor integrators [110-115]. With many of these techniques, the feedback path around the op-amp is broken during the transitions between phases. Matsumoto [116] has proposed an interesting variant on the technique, which features continuous feedback around the op-amp, producing a 'spike-free' output. These techniques would seem to be most applicable to GaAs processes, where the obtainable op-amp gain is low [117]. Similar techniques have been used to cancel or reduce the op-amp output offset voltage [118-121], clock feedthrough [121,122], and low frequency noise [123-125], all of which have presented problems in practice. Fully differential circuit topologies, which feature op-amps with differential outputs, have been shown to have advantages in noise performance, particularly in respect of power supply rejection, and high frequency performance [59,126,127]. In practical systems, the complexity of the pre-filtering and post-filtering requirements is such that decimation and interpolation techniques respectively [128] are often used to reduce the stringency of the continuous-time filtering requirement. Switched-capacitor circuits to achieve these functions have been proposed in [18,129-134].

In spite of all the progress that has been made in recent years, an

analysis by Gray and Castello of the theoretical limitations of switched- capacitor filters [135] shows that the current technology falls far short of reaching these limits. Thus there remains considerable scope for improvement in the performance of switched- capacitor filters.

2.5 Applications of SC Filters.

2.5.1 General Applications.

Switched-capacitor techniques have been employed in many applications. Programmable filters can be implemented using programmable capacitor arrays [136]. Early switched- capacitor filters had an indifferent noise performance, but excellent results were obtained by applying the technique of chopper stabilisation [137] to a fully differential design allowing a dynamic range in excess of 100dB to be achieved. This level of performance allows switched- capacitor filters to be used in pre-filter applications for the most demanding PCM specifications. Switched- capacitor filters have been used in PCM codecs [138,139] where they are used for anti-aliasing, post-filtering and hum rejection. The range of operating frequencies for switched- capacitor filters has been extended well beyond the voice-band range. Choi *et al.* presented a ladder-based elliptic bandpass filter with a clock frequency of 4 MHz and a centre frequency of 260 kHz, intended for AM IF applications [140]. Their results are particularly impressive in that a process with the conservative feature size of 4 μm was used to fabricate the filter. Matsui *et al.* [141] have constructed transversal switched- capacitor filters with a sampling rate of 14 MHz and 4 Mhz bandwidths for video applications. Tawfik and Senn have implemented lowpass switched- capacitor filters with 18 MHz sampling rates and a cutoff of 3.6 MHz using conventional ladder-based structures [142]. The same design team, with Assael, has also presented a silicon compiler for switched-capacitor filters [143].

2.5.2 Adaptive Filters and Equalisers

Another application in which switched- capacitor filtering technology has been used is line equalisation, i.e. compensating for the frequency characteristics of, typically, a telephone line. As early as 1981, Martin [144] had proposed circuits suitable for adaptive applications using switched- capacitor technology. However, the

earliest proposal for a line equaliser, by Suzuki *et al.* [145], used a different approach. A third order switched- capacitor filter was used, based on the biquad of [23], and clocked at four times the bit rate, to compensate for the line loss, and to bandlimit the signal so as to minimise inter-symbol interference. (Other circuitry was also proposed, not using the switched- capacitor technique, but required for the integration of this application, such as a digital PLL to synchronously lock the switched- capacitor filter operation to the incoming bit rate, and a decision feedback equaliser , to compensate for the effect of bridge taps (i.e. stubs) on Japanese and American telephone lines).

A crude form of adaptation was proposed, based on the level of the equaliser output signal. The switched- capacitor filter used contained programmable capacitor arrays and could be programmed to equalise various line lengths, the switched- capacitor filter setting being dictated by the equaliser output level. The switched- capacitor filter clock rate was 800 kHz, allowing an effective bidirectional data rate of 80 kb/s, at a line bit rate of 200 kb/s, using time compression multiplexing.

A more conventional adaptive equaliser based on the LMS algorithm was fabricated by NEC [146]. Standard switched- capacitor filter blocks of the type shown in Fig. 2.1 were not used. Instead, a four-quadrant analog multiplier formed the basis of the design. A cursory examination of the circuit for this multiplier indicates that its output voltage is grossly distorted, making the filtering technique used difficult to apply. Another adaptive finite impulse response filter was integratedby Fellman and Broderson [147]. However, it was intended for applications in speech processing rather than telecommunications.

Further circuits for performing arithmetic operations were proposed in [148]. The op-amps in these circuits are open-loop during transitions of the three phase clock, which obviously limits their operating speed.

The equaliser proposed by Suzuki in [145] was integrated on a 2.5 μm process in 1983 [149,150]. Interestingly, not all the capacitors in the switched-capacitor filter used are programmable, the fixed capacitors being such that, although the switched- capacitor filter transfer function is of third order, two of the filter poles are fixed, and cannot be programmed.

A similar but slightly more complex equaliser was designed by Nakayama *et al.* [151] at NEC on a 3 μm CMOS process. In the NEC design, the equaliser output is post-filtered so as to obtain a continuous-time waveform. This means that the switched- capacitor filter need not operate synchronously with the bit rate. A switched- capacitor filter called a roll-off filter is interposed between the equaliser output and the post-filter. No details of its design are given, although the stated purpose is to shape the equaliser output so as to minimise inter-symbol interference. The design is intended for the same application as in [145], i.e. digital data communication at a bit rate of 200 kb/s using time compression multiplexing, but contains no decision feedback equaliser. A similar equaliser, from the same design team, for four-wire full-duplex communication is described in [152].

The most complex of these early designs for line equalisers is that of Ishikawa *et al* [153], a block diagram of which is shown in Fig. 2.5. It is similar to that of [151], featuring non-synchronous operation, but includes a third order lowpass switched- capacitor filter clocked at twice the rate of the main equaliser section (i.e. at 1.6 MHz) in the prefilter, whose purpose is to act as a decimation stage. The roll-off filter is a fourth-order switched- capacitor low pass filter, clocked at the same higher rate, and thus acts as an interpolation stage. This simplifies the design of the continuous-time filters in the pre-filter and post-filter respectively. A decision feedback equaliser is also included. The programmable capacitor arrays are binary weighted and controlled by a ROM. Thus only integer values for the programmable capacitors are allowed. The bit rate is, as with the other designs, 200 kb/s and the equaliser is fabricated on a 2 μm process. Unlike the other authors, Ishikawa presents a flow-chart describing the adaptation algorithm. Another refinement in this design is the presence of an offset-cancelling stage at the equaliser output.

An equaliser using a fully differential architecture was described in [154]. It is intended for amplitude equalisation of voice signals and, although digitally programmable, is not in itself adaptive.

The operating frequency range of switched- capacitor line equalisers has recently been extended to allow operation at bit rates compatible with ISDN

requirements. Such an equaliser has been designed by Siemens for digital PABX applications [155]. The bit rate is 384 kb/s. The design is similar to that in [149] and operates synchronously, but is without a decision feedback equaliser, and features a decimating low pass filter at the equaliser input, like that of [153], of which, incidentally, no details are given. It is suitable for use only with short line lengths, presumably because longer line lengths require a higher bit rate to achieve a given bidirectional data rate using time compression multiplexing, due to the increased cable group delay. An adaptation algorithm is presented for the system which is more sophisticated than those for earlier designs, in that the gain and frequency response of the equaliser are adjusted separately. Thus the equaliser can be used with more than one line type. The equaliser is fabricated on a 2 μm CMOS process, and the highest switched- capacitor filter clock rate is 3.072 MHz (for the pre-filter).

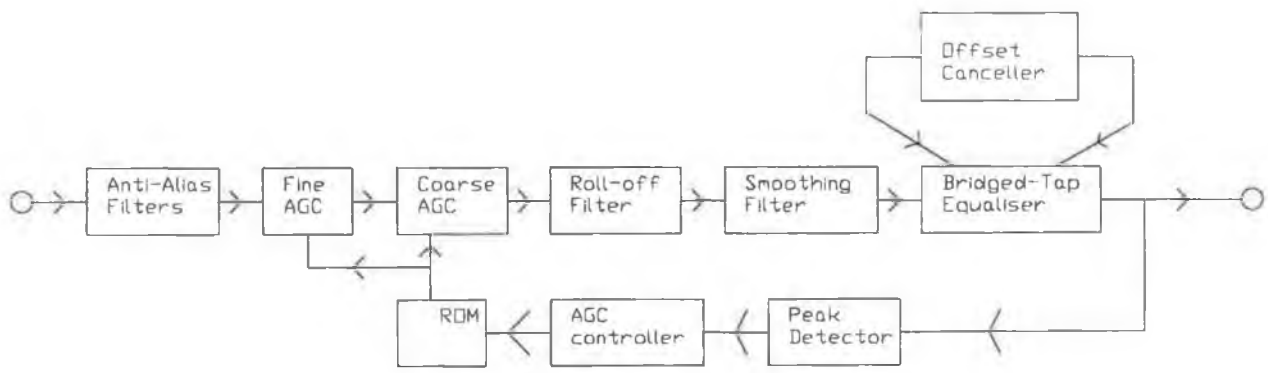


Fig. 2.5: Block Diagram of Adaptive Line Equaliser

The NEC design of [151] has been further improved to achieve compatibility with ISDN requirements [156]. The resulting system resembles that of [153] closely, but achieves a bit rate of 320 kb/s using a 3 μm process. To achieve this rate, the capacitance ratio spread had to be minimised by using a fourth order switched- capacitor filter to implement a third order transfer function, the redundant pole and zero cancelling, and being chosen so as to minimise the capacitance ratio spread.

The success of the approach described above to integrating a line equaliser may be judged by its adoption in some designs based on digital signal processing technology, even though fully adaptive digital filters can be readily designed [157-159].

Chapter Three: THE SYNTHESIS OF LDI-BASED SC FILTERS

3.1: Basic Concepts.

3.1.1: Stray-sensitive Circuits.

The first low pass switched- capacitor filters based on passive LC prototypes were of the type shown in Fig. 3.1 for the case of a third order filter. Using the principle of charge conservation [48], the difference equations describing the filter can readily be derived as

$$V_1(n+\tfrac{1}{2}) = (1-C_{31}/C_{21})V_1(n-\tfrac{1}{2}) + C_{11}/C_{21}(V_{in}(n)-V_2(n))$$

$$V_2(n) = V_2(n-1) + C_{12}/C_{22} (V_1(n-\tfrac{1}{2}) - V_3(n-\tfrac{1}{2}))$$

$$V_3(n+\tfrac{1}{2}) = (1-C_{33}/C_{23})V_3(n-\tfrac{1}{2}) + C_{13}/C_{23}\, V_2(n) \qquad (3.1)$$

where V(n) means the value of the voltage V(t) on the 'even' phase φ_2 i.e. from t = $(n-\frac{1}{2})T$ to t = nT, and where $V(n-\frac{1}{2})$ means the value of V(t) on the 'odd' phase φ_1, i.e. from t = (n-1)T to t = $(n-\frac{1}{2})T$, T being the clock period.

The difference equations can be transformed into the frequency domain to obtain (where $z = e^{sT}$)

$$\begin{aligned} V_1(z) &= T_1(z)\,(V_{in}(z) - V_2(z)) \\ V_2(z) &= T_2(z)\,(V_1(z) - V_3(z)) \\ V_3(z) &= T_3(z)\, V_2(z) \end{aligned} \qquad (3.2)$$

where

$$\begin{aligned} T_1(z) &= C_{21}/C_{11}\,(z^{1/2} - z^{-1/2}) + C_{31}/C_{11}\, z^{-1/2} \\ &= 2\, C_{21}/C_{11}\, \gamma \qquad\qquad + C_{31}/C_{11}\, z^{-1/2} \end{aligned}$$

$$\begin{aligned} T_2(z) &= C_{22}/C_{12}\,(z^{1/2} - z^{-1/2}) \\ &= 2\, C_{22}/C_{12}\, \gamma \end{aligned}$$

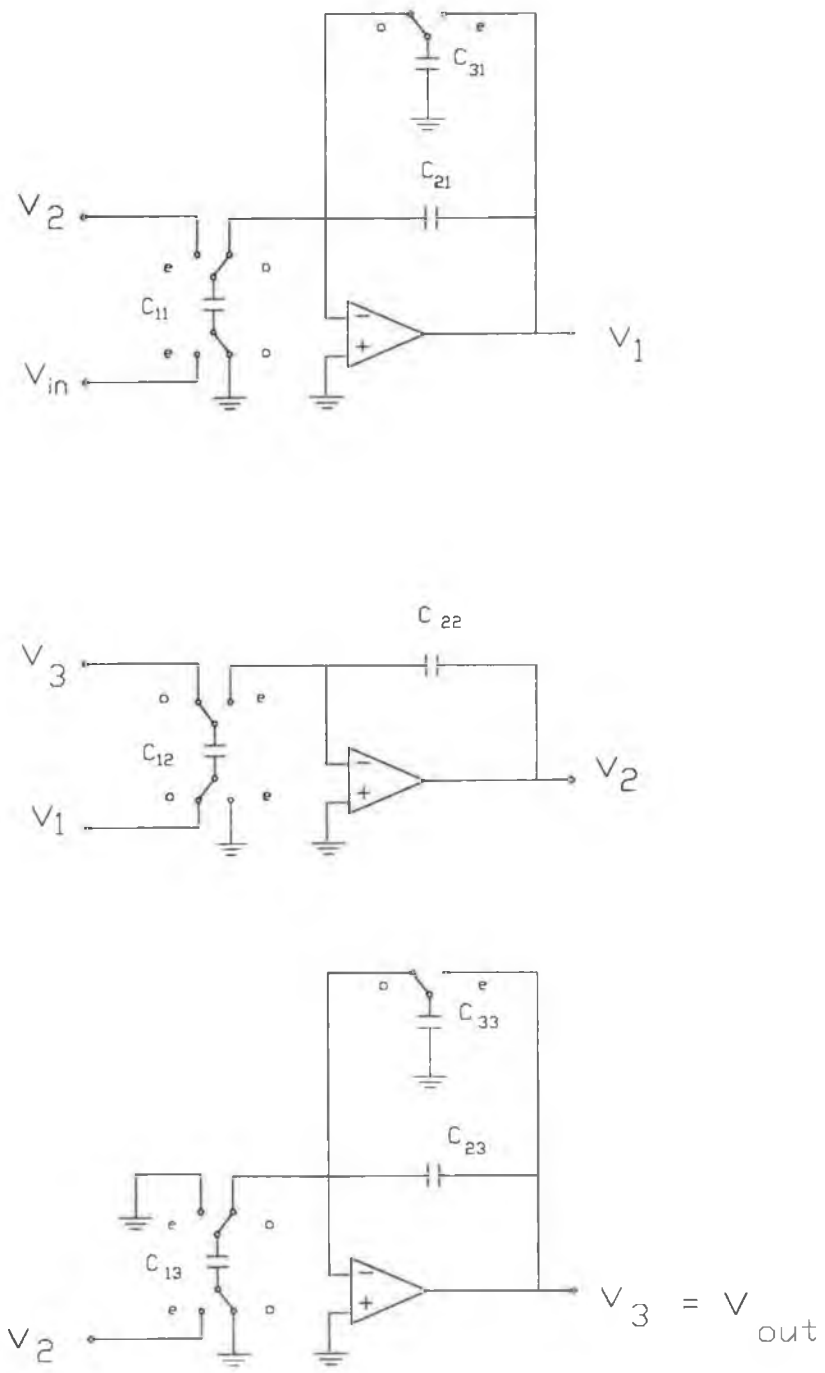


Fig. 3.1: Stray-sensitive SC ladder filter.

$$T_3(z) = C_{23}/C_{13}\,(z^{1/2} - z^{-1/2}) + C_{33}/C_{13}\,z^{-1/2}$$
$$= 2\,C_{23}/C_{13}\,\gamma + C_{33}/C_{13}\,z^{-1/2} \qquad (3.3)$$

and where γ is the linear discrete integration variable [10,76]

$$\gamma = \tfrac{1}{2}\,(z^{1/2} - z^{-1/2})$$
$$= \sinh(sT/2) \qquad (3.4)$$

This filter can be represented by the same signal flowgraph as the hypothetical passive ladder network shown in Fig. 3.2 where the equivalent element values are $R_S = C_{31}/C_{11}$, $R_1 = C_{33}/C_{13}$, $L_1 = 2\,C_{21}/C_{11}$, $C_2 = 2\,C_{22}/C_{12}$, and $L_3 = 2\,C_{23}/C_{13}$, and where the inductor currents and capacitor voltages are used as the state variables.

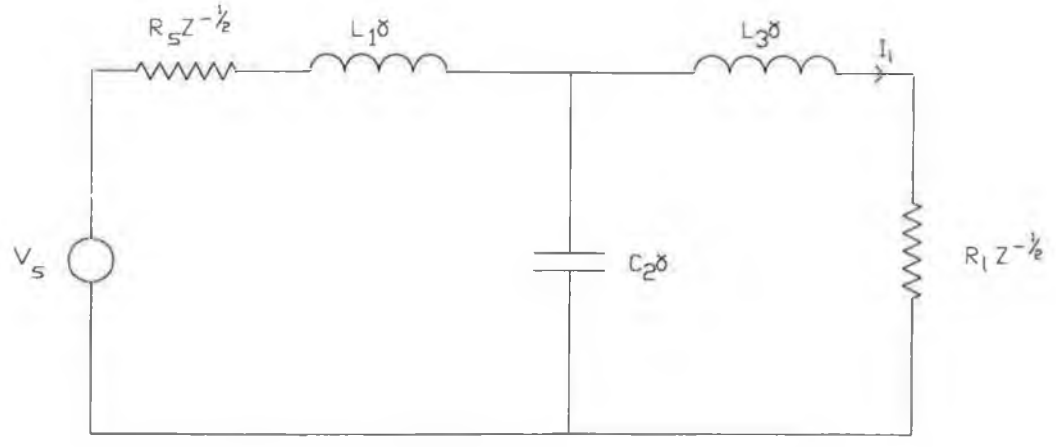


Fig. 3.2: Equivalent circuit of third order switched-capacitor lowpass ladder.

It is to be noted that standard techniques for the synthesis of ladder circuits, such as those due to Darlington, are not applicable to the synthesis of this network, because they apply to doubly-terminated ladders with frequency-independent terminations, whereas the terminations of this filter introduce a phase shift which varies with frequency.

The filter of Fig. 3.1 is often referred to as a switched-capacitor ladder, or l.d.i. ladder filter. This title is descriptive and convenient, although it is more accurate to call it a state-variable filter, or a switched- capacitor 'leapfrog' filter [76,160].

3.1.2: Stray-insensitive Circuits.

3.1.2.1: Integrator Circuits.

The integrator circuits of Fig. 3.1 are not used in modern filters because they are stray-sensitive [9]. Instead they have been replaced by the circuits of Fig. 2.1. Use of stray-insensitive building blocks is essential for practical switched capacitor filters. This is because such sections are designed so that stray capacitances between the capacitor plates and the substrate do not affect the charge transfer through the filter section. Filter sections without this property require a prohibitive area when integrated, since the capacitors must be large enough to minimise the effects of these stray capacitances, which are inevitably present when a filter is integrated. The success of the integrators of Fig. 2.1 in practice stems from their property of stray-insensitivity. However, the inverting circuit in Fig. 2.1 does not in fact implement the linear discrete integration correctly. A true l.d.i. based inverting integrator should implement the z-transform (in the sense that $z = e^{sT}$) equation

$$V_o(z) = - k\ V_{in}(z)/(z^{1/2} - z^{-1/2}) \tag{3.5}$$

which, written in the form of a difference equation, is

$$V_o(n) = V_o(n-1) - k\ V_{in}(n-\tfrac{1}{2}) \tag{3.6}$$

whereas the actual difference equation describing the operation of the

integrator is

$$V_o(n) = V_o(n-1) - k\ V_{in}(n) \qquad (3.7)$$

Thus, the problem is that the integrator does not introduce a delay of $T/_2$ in the signal path from the input to the output of the integrator, as is required for correct operation. This difficulty can be overcome by phasing the switches in a switched-capacitor simulation of a low-pass ladder in such a way that the required delay of $T/_2$ is introduced in the signal path. (For convenience, the undamped integrators of Fig. 2.1 shall be referred to as non-inverting and inverting LDIs, and the damped integrators as non-inverting and inverting DDIs, even though the operation of linear discrete integration may not in fact be performed exactly.)

3.1.2.2: Clock Phasing of Stray-insensitive Filters.

A number of topologies are possible for achieving the correct phasing, and these differ in the number of switches and capacitors required. However, if all components are ideal, it is found that all of these topologies yield the same transfer function as the basic stray-sensitive ladder. If it can be assumed that all circuit elements are ideal, then the only basis we have for selecting between these topologies is the number of switches and capacitors used. However, an analysis which takes account of non-ideal factors, such as finite op-amp gain and bandwidth and non-zero switch on-resistances, will generally reveal one of the topologies as being superior in a particular application.

Fig. 3.3 shows the first topology to be considered. This uses the building blocks of Fig. 2.1. Where two switches in the resulting filter perform the same function, only one switch need be used, a technique known as switch sharing. Thus S_{3a}, S_{3b}, and S_{3c} can be replaced by a single switch S_3. This circuit differs from the standard leapfrog topology of Fig. 3.1 in that it uses sections whose output is related to the sum of their inputs, rather than to the difference. Thus they do not directly simulate the voltages or currents in an LC ladder. Instead the approach taken is to alternate sections with inverting and non-inverting outputs. It can be shown, for example by using flowgraphs, that this results in the output of every second filter stage differing from the corresponding

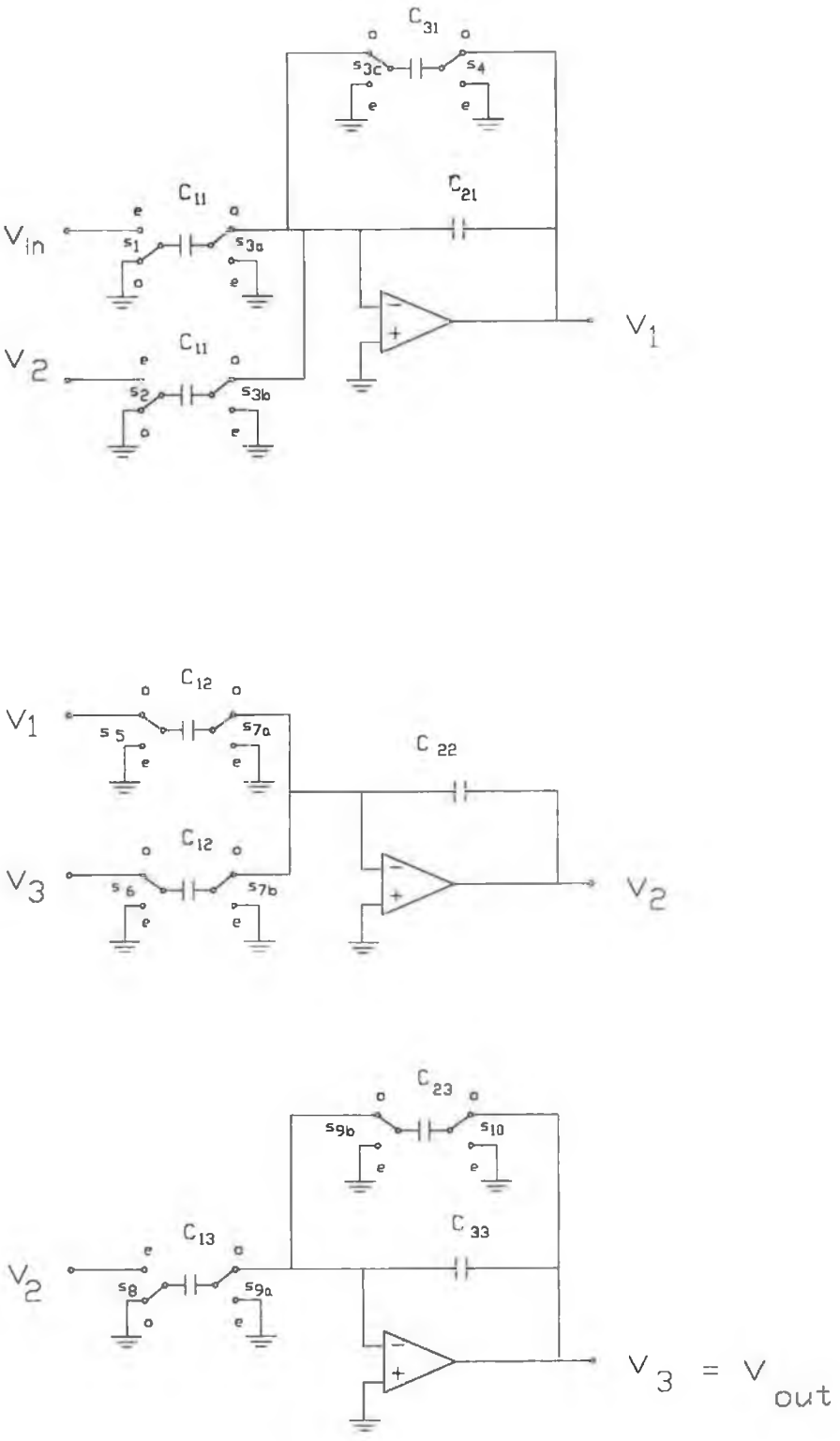


Fig. 3.3: Third order stray-insensitive SC ladder.

LC ladder current or voltage, which it is supposed to be simulating, by a factor of - 1, with all other outputs unchanged. Thus the form of the filter transfer function is directly analogous to that of an LC ladder for even order filters and differs only in being inverted in an odd order filter. The manner in which the effect of the delay-free operation of an inverting LDI is compensated for in the operation of this circuit will now be described.

The circuit of Fig. 3.3 contains a non-inverting DDI as the first section, then an inverting LDI, and the last section is again a non- inverting DDI. The DDIs introduce a delay of $T/_2$ seconds, in that the output is not affected by the input until $T/_2$ seconds after the input is sampled. However the topology, and switch phasing, is such that the outputs of all the sections are updated simultaneously. Thus the DDI inputs are updated $T/_2$ seconds before they are sampled, and so the effective delay through these sections is T seconds, $T/_2$ seconds more than for a standard stray-sensitive DDI. In contrast, the second section contains a delay of zero, i.e. $T/_2$ seconds less than for the standard type. If we model the filter as a ladder, then it is equivalent to impedance scaling an exact LDI type ladder by $z^{1/2}$. Thus, we would expect the output to be delayed, with respect to that which would obtain for a standard LDI filter, by $T/_2$ seconds, whilst the amplitude response would be identical. In fact, the correspondence between this filter and the original is exact, since the above discussion has assumed that there is a delay of $T/_2$ seconds between the time at which the inputs to the first stage are updated, and the time at which they are sampled, whereas in fact one of those inputs, the input signal, is (assumed to be) continuous. Thus there is no additional delay of $T/_2$ seconds. The delays through the filter are shown in Table 3.1, where time t = nT represents the even phase φ_2, and where t = $(n-\frac{1}{2})T$ co-incides with the odd phase φ_1.

Stage:	O/p at:	I/ps read:	I/ps updated:	Overall delay:
1	$(n+\frac{1}{2})T$	nT	$(n-\frac{1}{2})T$ (V2 only)	T ($T/_2$ for Vin)
2	$(n+\frac{1}{2})T$	$(n+\frac{1}{2})T$	$(n+\frac{1}{2})T$	0
3	$(n+\frac{1}{2})T$	nT	$(n-\frac{1}{2})T$	T

Table 3.1 : Filter section delays for Fig. 3.3.

After sharing S_{3a}, S_{3b}, and S_{3C} as S_3, sharing S_{7a}, S_{7b}, and S_{7C} as

S_7, and sharing S_{9a}, S_{9b}, and S_{9c} as S_9, the filter in Fig. 3.3 requires ten capacitors and ten switches, i.e. two more switches, and two more capacitors, than required by the stray-sensitive filter. However, considering the first filter stage, the equivalent inductance in Fig. 3.2 is $L = 2(C_{21}+C_{31})/C_{11}$, compared with $L = 2C_{21}/C_{31}$ for the corresponding stage in Fig. 3.1, while the resistance $R_S = C_{31}/C_{11}$ is unchanged. Thus the value of C_{21} (and by an identical argument, of C_{23}) required is less for this type of filter (and similarly for all filters based on the circuits of Fig. 2.1) than for the stray-sensitive type, for a given value of C_{11} (C_{13}). One disadvantage of this filter is that each section, except the final one, requires two capacitors of equal value at the input, and any mismatch would presumably affect performance, since it would introduce an additional sensitivity term not present in the original prototype ladder. A second disadvantage is that, on φ_2, the three op-amps are interconnected. This results in a network that takes longer to settle than alternative structures, resulting in inferior high frequency performance [59].

The number of switches used by this filter can be further reduced by noting that some are redundant. For example, S_2 switches between V_2 and ground, as does S_8. Thus S_8 can be eliminated, and the input to the third section can be taken from S_2. Similarly S_5 and S_{10} can be eliminated, as being equivalent to S_4 and S_6 respectively. Thus the number of switches required can be reduced to seven.

If the phases on the switches in the second section are reversed, then we get the filter shown in Fig. 3.4. Again we get the same transfer function, but this time each filter section has a delay of $T/_2$, so that each section implements an exact LDI or DDI. This is shown in Table 3.2.

Stage:	O/p at:	I/ps read:	I/ps updated:	Overall delay:
1	$(n+\frac{1}{2})T$	nT	nT	$T/_2$
2	nT	nT	$(n-\frac{1}{2})T$	$T/_2$
3	$(n+\frac{1}{2})T$	nT	nT	$T/_2$

Table 3.2. Filter section delays for Fig. 3.4.

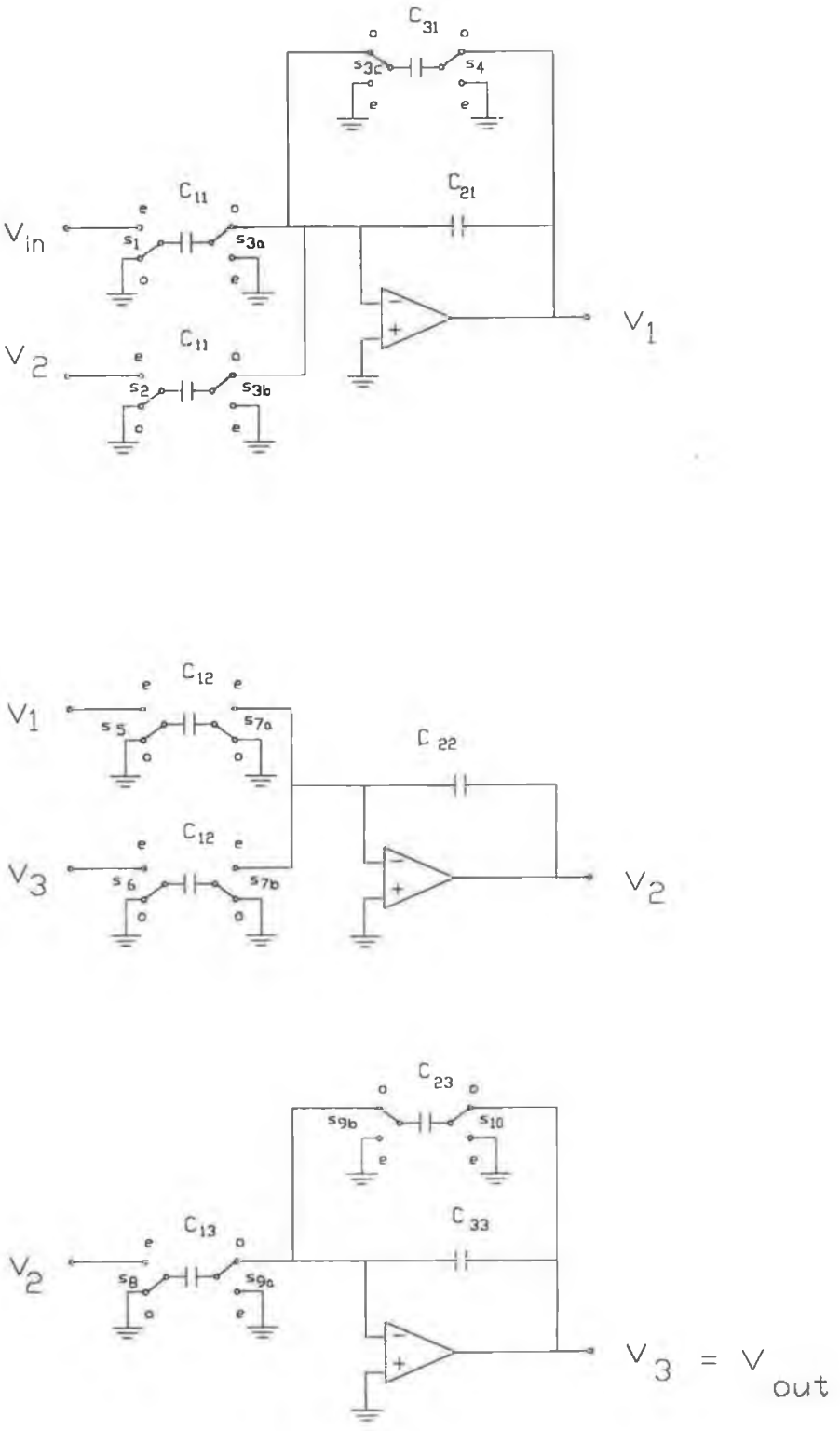


Fig. 3.4: Third order stray-insensitive SC ladder.

The disadvantage of this topology is that now, apart from S_3, S_7 and S_9, only S_2 and S_8 can be shared, so that a minimum of nine switches and ten capacitors are required.

A number of variations in the switching schemes for the above filters are possible. For example, by reversing the phases on S_1 in Fig. 3.3, we ensure that V_{in} is sampled during the same phase at which V_2 is updated, and so there will be an extra delay of $T/_2$ seconds through the filter. Also the resulting input section will have a differential input, and so V_{in} will be inverted by it. Another variation is to use an inverting DDI as the first section, and then to alternate inverting and non-inverting sections as before. It is evident that, assuming ideal components, there will be no variation in the amplitude of the frequency response among these filter types.

It is also possible to use sections with differential inputs to implement a stray-insensitive LDI ladder. However, because it is not possible to design an inverting stray-insensitive LDI section which includes a delay using circuits of the type in Fig. 2.1, such differential input sections will not sample their two inputs simultaneously. Hence, it is necessary to ensure that the two inputs are updated simultaneously in order to implement LDI- type integration correctly. Fig. 3.5 shows one possible arrangement. The operation of this filter is clarified in Table 3.3.

Stage	1	2	3
Output available:	$(n+\frac{1}{2})T$	nT	$(n+\frac{1}{2})T$
(+) i/p sampled:	nT	$(n+\frac{1}{2})T$	nT
(+) i/p available:	continuously	$(n+\frac{1}{2})T$	nT
(-) i/p sampled:	$(n+\frac{1}{2})T$	nT	--
(-) i/p available:	nT	$(n+\frac{1}{2})T$	--
Overall delay:	$T/_2$	$T/_2$	$T/_2$

Table 3.3 : Delays in the circuit of Fig. 3.5.

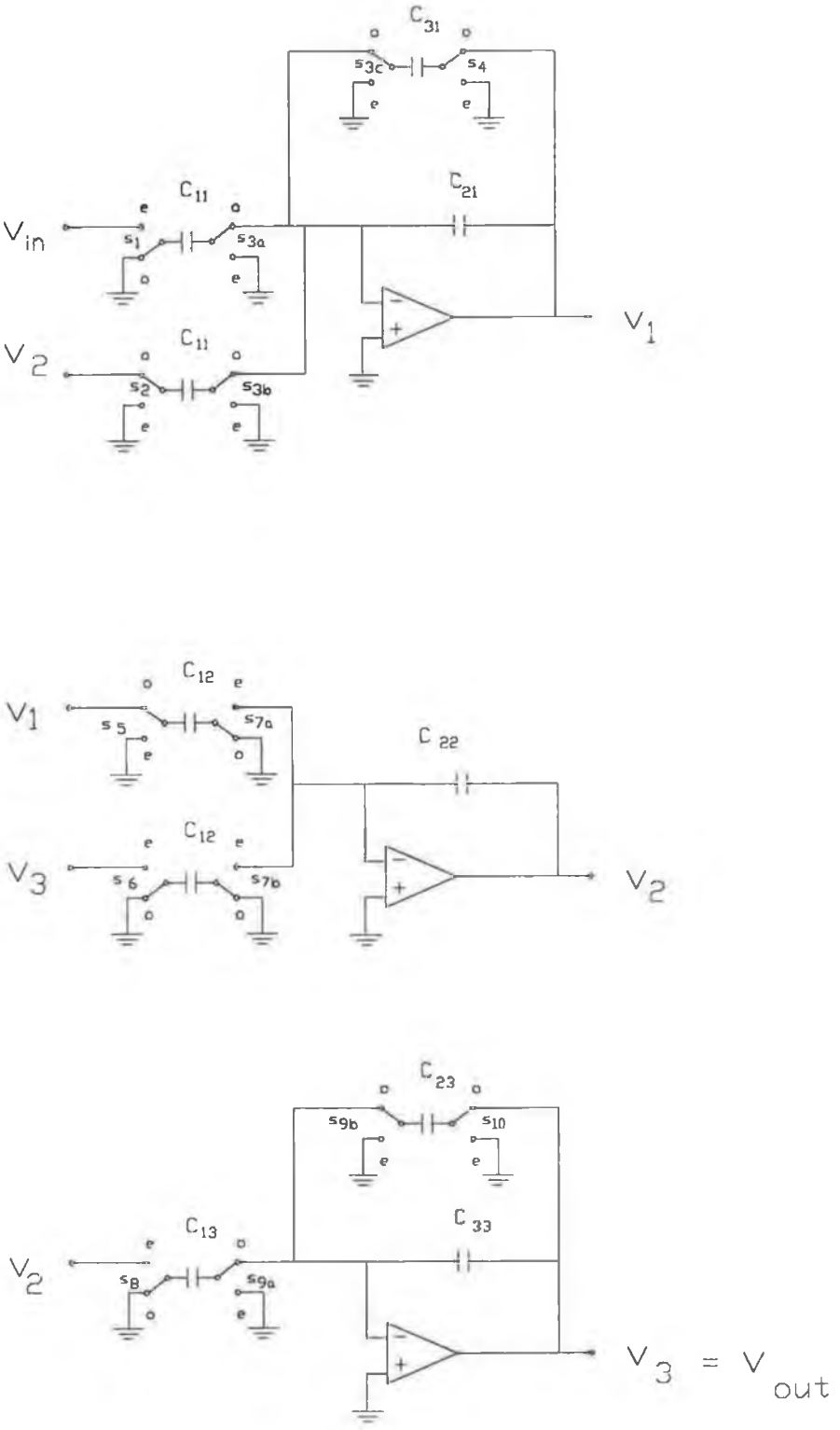


Fig. 3.5: Third order stray-insensitive SC ladder.

Apart from the usual S_3, S_7, and S_9, only S_4 and S_5 can be shared for this topology, so that again nine switches and ten capacitors are required.

The topology requiring the minimum number of switches and capacitors is probably that shown in Fig. 3.6. This again uses a differential structure, but exploits the fact that the inputs are read alternately in order to eliminate one of the two input capacitors for each section, as well as one of the corresponding switches. The delays for this topology are shown in Table 3.4.

Stage	1	2	3
O/p available:	$(n+\frac{1}{2})T$	nT	$(n+\frac{1}{2})T$
(+) i/p sampled:	nT	$(n-\frac{1}{2})T$	nT
(+) i/p available:	cont.	$(n-\frac{1}{2})T$	nT
(-) i/p sampled:	$(n+\frac{1}{2})T$	nT	--
(-) i/p available:	nT	$(n-\frac{1}{2})T$	--
Overall delay:	$T/_2$	$T/_2$	$T/_2$

Table 3.4 : Delays in the circuit of Fig. 3.6.

In this topology no switches other than the pair of C_3 capacitors and of C_9 capacitors can be shared. However only eight switches and eight capacitors are required. Therefore there is no penalty in terms of the number of such components for using this structure in preference to the stray-sensitive circuit of Fig. 3.1.

Various types of stray-insensitive topology for an LDI ladder filter have been discussed above. Assuming ideal components, the type shown in Fig. 3.6 is obviously to be preferred. However, a simulation which allowed for non-ideal components might reveal the performance of one of the other types to be superior. For example, it might reveal that the fact that the two inputs to each integrator are sampled at different times results in a high-frequency response that deteriorates more rapidly than for some of the other topologies, or that the sharing of switches results in excessive charging times for the associated capacitors. Considerations of such non-ideal operation must be investigated, where possible, for any particular application, by using simulations with parameters relevant to the fabrication process

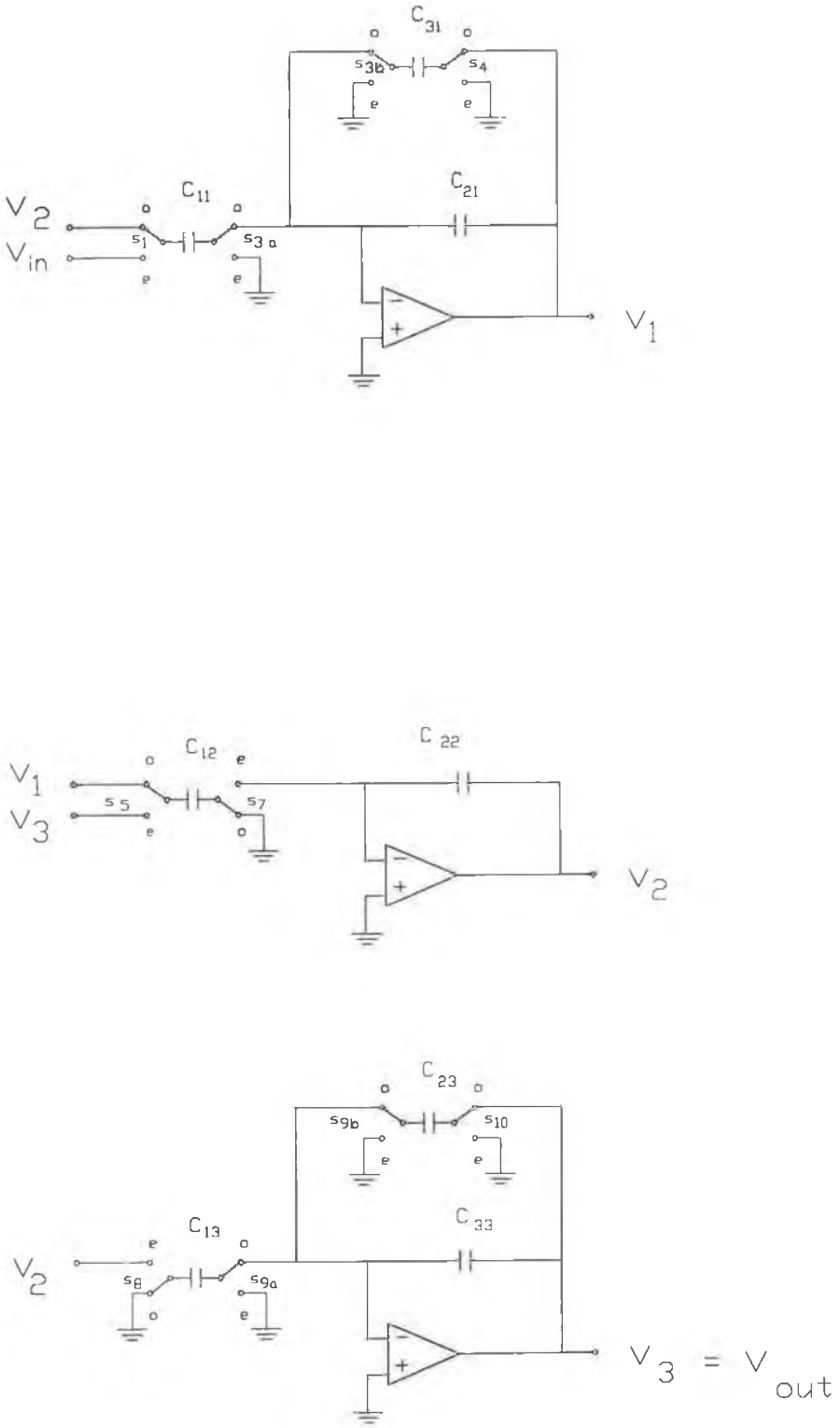


Fig. 3.6: Third order stray-insensitive SC ladder.

being employed, and the topology which is most robust in the face of the non-idealities of the process being used should be selected.

3.2: An Exact Design Procedure.

3.2.1: Stability

The analysis above, which can be repeated with similar results for a filter of arbitrary order, indicates that the so-called switched-capacitor ladder filters accurately simulate a passive LC lowpass ladder, except that the variable 's' is mapped to the variable 'γ', and the terminations, which have constant resistances R_S and R_l in the prototype ladder, vary with frequency as $R_S z^{-1/2}$ (for even and odd order filters) and $R_l z^{-1/2}$ (for odd order filters) in the equivalent circuit of the switched-capacitor ladder. For even order filters, the equivalent circuit of the final filter stage (whose output voltage represents a current in the prototype filter) is an admittance, rather than an impedance, and so the conductance of the output termination varies with frequency as $G_l z^{-1/2}$.

If the terminations did not vary with frequency, the resulting filter would be unconditionally unstable [10,76] since, for every pole of the filter response in the γ- plane, there would be two poles in the z-plane, one inside and one outside the unit circle, because the value of γ (as a function of z) is unaffected if $-z^{-1}$ is substituted for z. Thus, if the reactances in the circuit vary with γ instead of with the Laplace variable s, then frequency variable terminations are necessary (although not sufficient) for a stable filter realisation. A new synthesis technique is required for these filters, because the standard techniques for the design of LC ladder filters assume frequency independent terminations. The solution to this problem presented by Scanlan [76] will now briefly be described.

3.2.2: Exact Analysis.

The first step in the design of such filters is to choose an approximation to the ideal lowpass filter to be realised. However, this assumes a knowledge of the general form of the filter transfer function which can be realised by the SC ladder topology. Thus an expression is necessary for the transfer function of the SC ladder.

To facilitate the analysis Scanlan considered the frequency variation of the terminations to be of the form $R\mu$ rather than $Rz^{-1/2}$, where $\mu = \frac{1}{2}(z^{1/2}+z^{-1/2}) = \cosh(sT/2)$. This is more appropriate as a choice of variable to represent the frequency variation of the terminations since μ is real for imaginary s (so the impedance of the terminations is purely resistive) unlike the earlier case. Making this change to the equivalent circuit of the SC filter results in only two changes in the equivalent circuit element values, namely the values of the reactances in the termination branches. Thus, for example, it iis easy to show that the impedance $R_S z^{-1/2} + L_1\gamma$ is equal to $R_S\mu + L_1'\gamma$ where $L_1' = L_1 - R_S$.

Consider the equivalent circuit of the odd order SC filter. This is shown in Fig. 3.7(a). The transfer function of the filter is $H_{21} = i_1/v_S$ since the final SC stage simulates an impedance. Impedance scaling by $1/\mu$ eliminates the frequency variation of the terminations. The resulting network, named by Scanlan the *auxiliary* network, is shown in Fig. 3.7(b). The voltage transfer function v_1/v_S is unaffected by the impedance scaling [74] so (representing variables associated with the auxiliary network in italics)

$$\frac{v_1}{v_S} = \frac{v_1}{v_S}$$

but

$$v_1 = \mu R_1 i_1 \quad , \quad v_1 = R_1 i_1$$

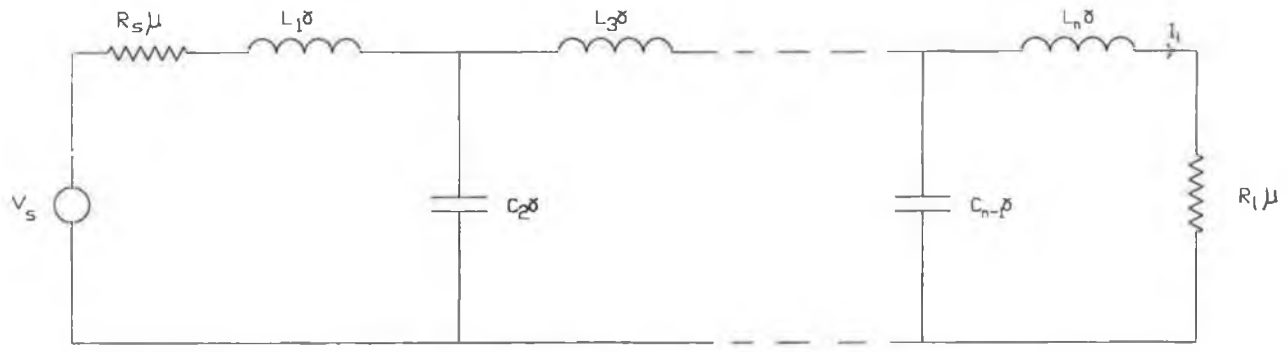
and so

$$v_1/v_S = \mu R_1 H_{21} \quad , \quad v_1/v_S = R_1 H_{21}$$

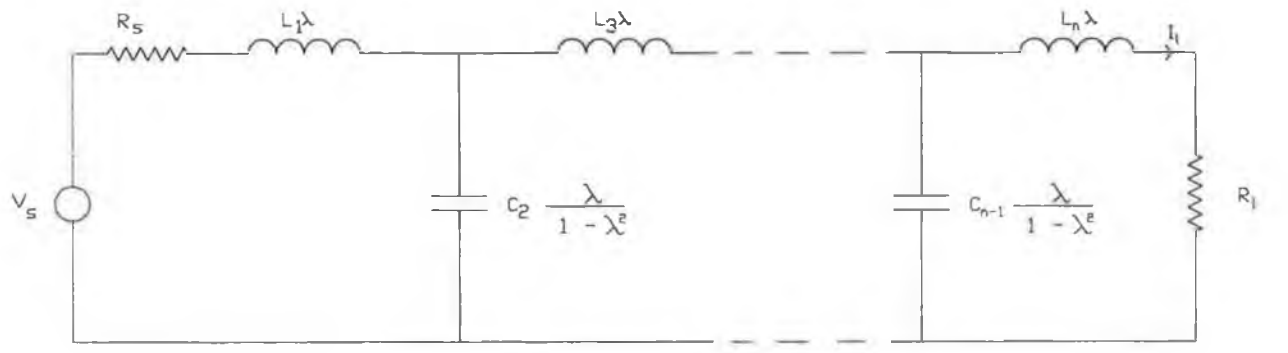
so

$$H_{21} = \mu H_{21}$$
$$= (1 - \lambda^2)^{1/2} H_{21} \qquad (3.8)$$

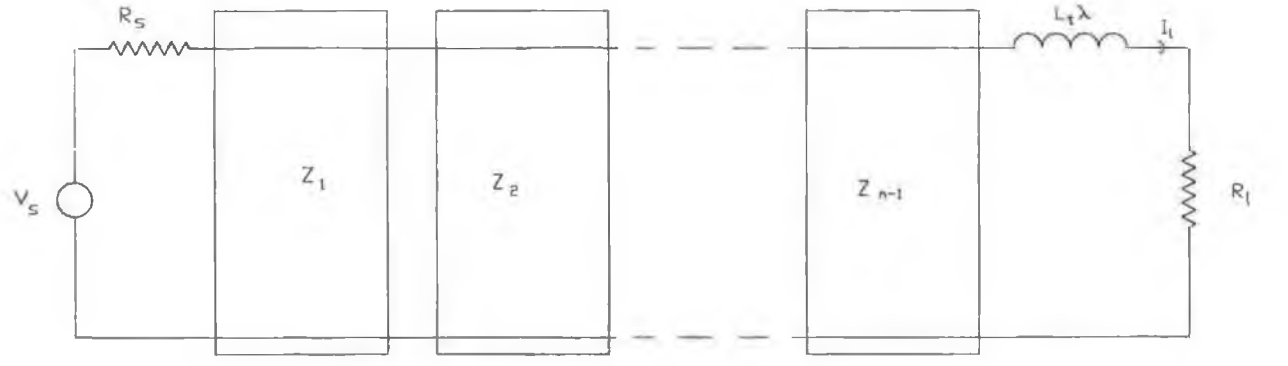
where $\lambda = \gamma/\mu = \tanh(sT/2)$ is the bilinear variable [10,161]. The impedance of the 'inductors' of Fig. 3.7(b) varies with frequency as $Z = L\lambda$. This impedance



(a): Equivalent Circuit.



(b): Auxiliary network.



(c): Alternative representation of auxiliary network.

Fig. 3.7: Odd-order SC ladder.

is equivalent to that of a short/circuit stub in a distributed network, in which context λ is known as Richard's variable [82]. The admittance of the 'capacitors' varies as $Y = C\lambda/(1 - \lambda^2)$ since $\gamma\mu = \lambda/(1-\lambda^2)$.

Scanlan has pointed out that the networks in Fig. 3.8(a) are equivalent, where Z_1 and Z_2 are unit elements [76]. Thus the circuit of Fig. 3.7(c) is exactly equivalent to that of Fig. 3.7(b). Fig. 3.7(c) represents a cascade of n-1 unit elements followed by a series s/c stub, which is known [74,82] to have a transfer function of the form :

$$H_{21} = \frac{(1 - \lambda^2)^{(n-1)/2}}{D_n(\lambda)} \tag{3.9}$$

so

$$H_{21} = H_{21}/\mu = \frac{(1 - \lambda^2)^{n/2}}{D_n(\lambda)} \tag{3.10}$$

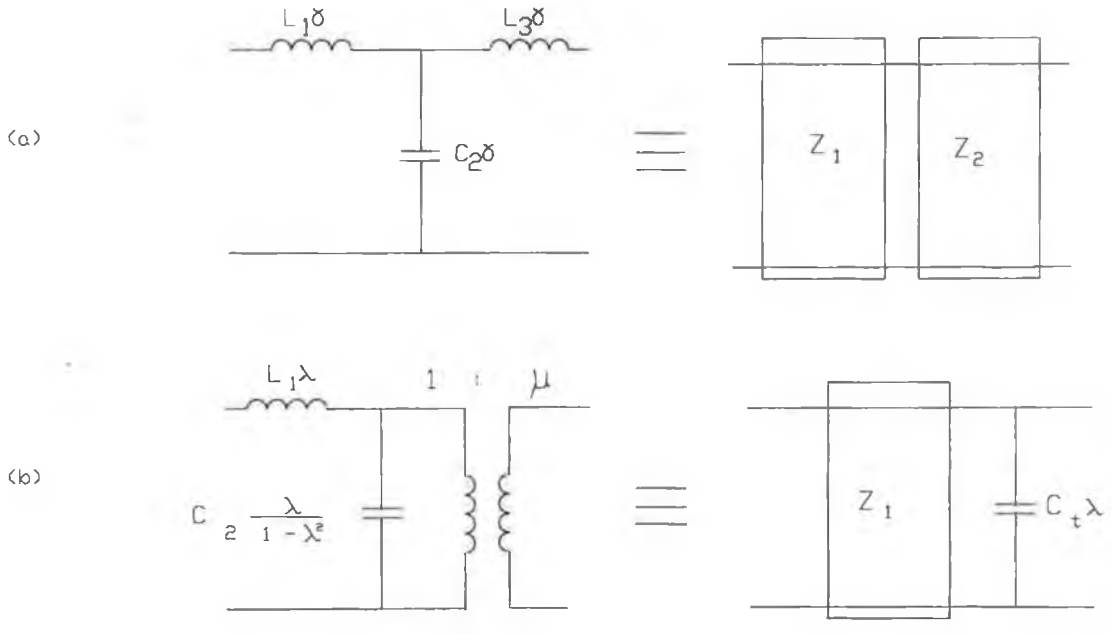


Fig. 3.8: Circuit equivalences used.

with $D_n(\lambda)$ an n-th order polynomial in λ. It follows from the properties of unit element filters [74] that if all the elements in Fig. 3.7(c) have positive values, the auxiliary network will be stable. Thus the original equivalent circuit, and consequently the switched- capacitor filter itself, will be stable, since the factor $1/\mu$ does not introduce instability.

Next the equivalent circuit of the even order filter, shown in Fig. 3.9(a), is considered. Again impedance scaling by $1/\mu$ results in the auxiliary network of Fig. 3.9(b). In the absence of the transformer at the output side of the network, and with a load of admittance $G_1\mu^2$ as would then be required, the transfer functions of the equivalent circuit and the auxiliary network would be the same. The introduction of the transformer, to allow a frequency independent termination, results in

$$H_{21} = \mu H_{21}$$

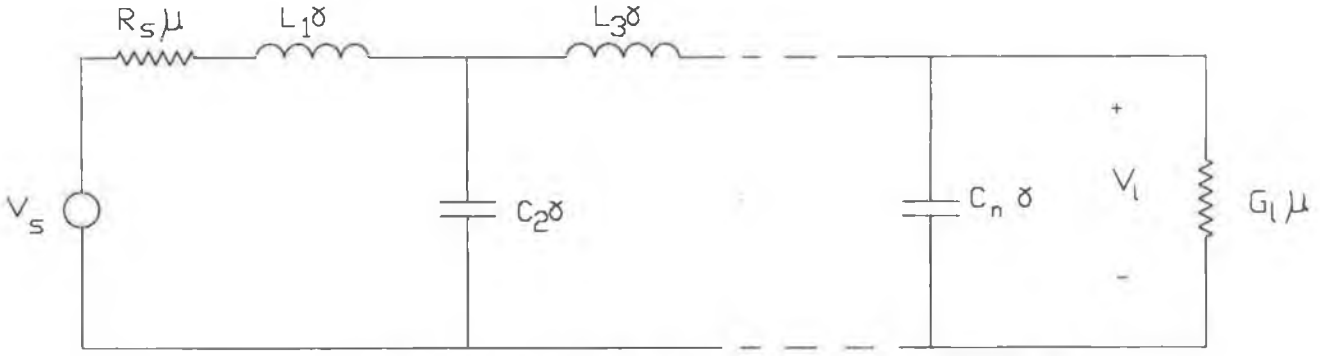
The identity of Fig. 3.8(a) is used to replace all but the last inductor-capacitor combination, and the output transformer by unit elements. The remaining components, shown in Fig. 3.8(b), are equivalent to a unit element followed by a shunt o/c stub, as proved by Scanlan. Thus Fig. 3.9(b) is equivalent to Fig. 3.9(c) which is known to have a transfer function of the form of (3.9), and thus the original switched- capacitor circuit has a transfer function of the same form as (3.10).

3.2.3: Low-pass Approximation Functions.

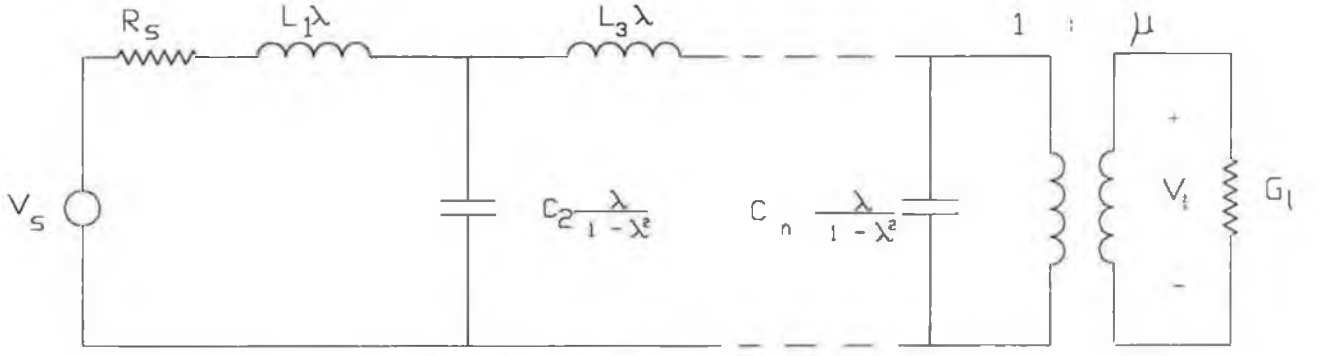
Having analysed the filter, the form required of the low-pass filter approximation can now be derived. Clearly

$$H_{21}(\lambda)H_{21}(-\lambda) = \frac{(1 - \lambda^2)^n}{D_n(\lambda)D_n(-\lambda)} \qquad (3.11)$$

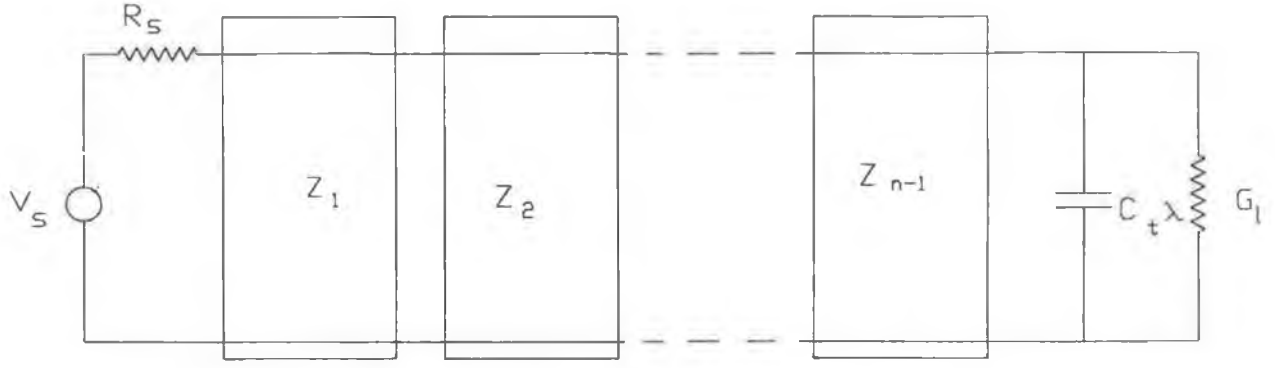
To find the response at physical frequencies, this is evaluated at $\lambda = j\Omega$, where $\Omega = \tan(\theta)$, $\theta = \pi f/f_s$, and $f_s = 1/T$ is the sampling rate. So



(a): Equivalent Circuit.



(b): Auxiliary network.



(c): Alternative representation of auxiliary network

Fig. 3.9: Even-order SC ladder.

$$|H_{21}(\theta)|^2 = \frac{(1 + \Omega^2)^n}{D_n(j\Omega)\ D_n(-j\Omega)} \qquad (3.12)$$

The denominator of (3.12) is of the form $F_n(\Omega^2)$ where $F_n(x)$ is an n-th order polynomial in x. The substitution $\Omega^2 \rightarrow \sin^2(\theta)\ /(1 - \sin^2(\theta))$ can now be made, to obtain

$$|H_{21}(\theta)|^2 = 1/F_n(\sin^2(\theta)) \qquad (3.13)$$

where $F_n(x)$ is an n-th order polynomial in x. One transfer function of this form is

$$|H_{21}(\theta)|^2 = K/(1 + G_n^2(\sin(\theta)) \qquad (3.14)$$

where $G_n(x)$ is an n-th order polynomial in x which is even or odd.

For a passband which is maximally flat at the origin, G_n is given by

$$G_n(\sin(\theta)) = \left[\frac{\sin(\theta)}{\sin(\theta_0)}\right]^n \qquad (3.15)$$

and for an equiripple passband, is given by

$$G_n(\sin(\theta)) = \epsilon T_n\left[\frac{\sin(\theta)}{\sin(\theta_0)}\right] \qquad (3.16)$$

where $T_n(x)$ is the n-th order Chebyshev polynomial of the first kind and $\theta_0 = \pi f_0/f_s$, f_0 being the desired filter cutoff frequency. The approximation functions are thus the same as those used for an LC low-pass passive ladder, but with the argument (ω/ω_0) replaced by $\sin(\theta)/\sin(\theta_0)$.

3.2.4: Synthesis.

The filter can now be designed by synthesising the auxiliary network. Since the terminations, for that network, are frequency-independent, the classical Darlington synthesis algorithm can be applied. The element values in the equivalent

circuit of the switched- capacitor filter are identical to those of the auxiliary network, and the capacitor ratios for the switched- capacitor realisation of the filter can thus be readily obtained from the auxiliary network element values.

The required form of $|H_{21}(\sin(\theta))|^2$ is chosen. So

$$|H_{21}|^2 = (1 + \Omega^2)^{-1} |H_{21}|^2 \tag{3.17}$$

It can be shown that the transducer power gain for the equivalent circuits in Fig. 3.7(a) and Fig. 3.9(a) are given by

$$|S_{21}|^2 = 4\ R_S(R_l)^k\ |H_{21}|^2 \tag{3.18}$$

where k = 1 for odd order filters, and k = -1 for even order filters. This is expressed as a rational function of Ω^2 and by analytic continuation ($\Omega^2 \rightarrow -\lambda^2$) the function $S_{21}(\lambda)S_{21}(-\lambda)$ is obtained. Hence $S_{11}(\lambda)S_{11}(-\lambda)$ is calculated as

$$S_{11}(\lambda)S_{11}(-\lambda) = 1 - S_{21}(\lambda)S_{21}(-\lambda) \tag{3.19}$$

The poles and zeros of $S_{11}(\lambda)S_{11}(-\lambda)$ are obtained. The left-half plane poles are appropriated to $S_{11}(\lambda)$ since stability requires that all the poles in the λ-plane occur where $\mathrm{Re}\lambda < 0$ [74,76]. For a minimum phase realisation, the left-half plane zeros are also assigned to $S_{11}(\lambda)$. There is a sign ambiguity in the value of $S_{11}(\lambda)$, since the value of $S_{11}(\lambda)S_{11}(-\lambda)$ is independent of the sign of $S_{11}(\lambda)$, corresponding to dual ladder realisations. To comply with the form of the equivalent networks chosen to represent the switched -capacitor filters in [76], the sign of $S_{11}(\lambda)$ is chosen to result in a pole at infinity in the input impedance.

The auxiliary network input impedance is formed as

$$Z_{in}(\lambda) = \frac{1 - S_{11}(\lambda)}{1 + S_{11}(\lambda)} \tag{3.20}$$

Richard's Theorem [82] is applied n-1 times to extract n-1 unit elements. The remaining stub is then extracted. Hence values are obtained for the elements of the auxiliary network, and so for the equivalent circuit of the switched- capacitor filter. The required capacitance ratios can then be obtained.

3.3: Practical Implementation of the Design Technique.

Software has been written to automate the above design procedure. Details of the algorithms used are given below.

3.3.1: Obtaining the input impedance.

The filter order n, sampling frequency f_s, cutoff frequency f_0, approximation type, and passband ripple (if required) are entered interactively. The co-efficients of the numerator and denominator λ-plane polynomials describing $S_{11}(\lambda)S_{11}(-\lambda)$ are then evaluated as follows :

For the maximally flat approximation:

$$S_{11}(\lambda)S_{11}(-\lambda) = \frac{-\lambda^2(1-\lambda^2)^{n-1} + \sin^{-2n}\theta_0(-\lambda^2)}{(1-\lambda^2)^n + \sin^{-2n}\theta_0(-\lambda^2)^n} \qquad (3.21)$$

where $\theta_0 = \pi f_0/f_s$. The co-efficients of terms like $(1-\lambda^2)^n$ are evaluated using the binomial theorem. The above expression follows directly from (3.15) and (3.19), upon using the substitution

$$\sin^2\theta \rightarrow -\lambda^2/(1-\lambda^2).$$

For the equiripple passband approximation:

First an expression is obtained for a polynomial which is denoted by $G_n(\lambda^2)$, and which is the numerator of $T_n^2(\sin\theta/\sin\theta_0)$, when expressed as a rational function of λ^2, using the above substitution. This is obtained as follows:

Calculate the co-efficients of $T_n(x)$, the Chebyshev polynomial of the first kind of order n, using the appropriate recursive definitions [162].

Hence obtain

$$T_n^2(x) = \sum_{0}^{n} a_i \, x^{2i} \tag{3.22}$$

Then

$$G_n(\lambda^2) = \sum_{0}^{n} g_k \, \lambda^{2k} \tag{3.23}$$

where

$$g_k = (-1)^k \sum_{i=0}^{n} a_i \, \sin^{-2i}(\theta) \begin{bmatrix} n-i \\ n-k \end{bmatrix} \tag{3.24}$$

The expression for $S_{1,1}(\lambda)S_{1,1}(-\lambda)$ is then

$$S_{1,1}(\lambda)S_{1,1}(-\lambda) = \frac{-\lambda^2(1-\lambda^2)^{n-1} + \epsilon^2 \, G_n(\lambda^2)}{(1-\lambda^2)^n + \epsilon^2 \, G_n(\lambda^2)} \tag{3.25}$$

where ϵ is related to the ripple specification by

$$10^{-r/10} = 1/(1 + \epsilon^2)$$

The poles and zeros of $S_{1,1}(\lambda)S_{1,1}(-\lambda)$ are then obtained using a rootfinding routine for polynomials available in the FORTRAN IMSL library of mathematical routines [163]. The co-efficients of $S_{1,1}(\lambda)$ are then found by the following method:

All the poles and zeros in the right-half λ-plane (i.e. those with positive real components) are discarded. If imaginary axis roots are found, then these should be of second order, allowing one to be discarded, and should occur in complex conjugates, otherwise $S_{1,1}(\lambda)$ will not have real co-efficients. This check for imaginary axis poles and zeros is included for generality only, since no such roots occur when using the approximations of (3.15) and (3.16).

Conjugate roots are assembled into second-order expressions, of the form $\lambda^2 - 2\mathrm{Re}[a] + |a|^2$. Real roots are assembled into first order factors of the form λ-a. The product of all the second-order and first-order terms is obtained for both the numerator and denominator of $S_{1,1}(\lambda)$ to obtain polynomials $N_{1,1}(\lambda)$ and $D_{1,1}(\lambda)$ respectively where

$$S_{11}(\lambda) = \pm N_{11}(\lambda)/D_{11}(\lambda).$$

The input impedance of the auxiliary network is then calculated as

$$Z_{in}(\lambda) = \frac{D_{11}(\lambda) + N_{11}(\lambda)}{D_{11}(\lambda) - N_{11}(\lambda)} \tag{3.26}$$

This corresponds to (3.20), with the sign of $S_{11}(\lambda)$ chosen such that the numerator polynomial of $Z_{in}(\lambda)$ is one degree higher in order than the denominator polynomial.

3.3.2: Synthesis of the Auxiliary Network.

Richard's Theorem [82] is applied n-1 times to Z_{in} to extract n-1 unit elements, using the technique described below:

Evaluate $Z_1 = Z_{in}(\lambda=1)$. This is the value of the extracted unit element.

Calculate the input impedance of the network obtained after extracting the unit element as

$$Z'_{in}(\lambda) = Z_1 \frac{N_Z(\lambda) - \lambda Z_1 D_Z(\lambda)}{Z_1 D_Z(\lambda) - \lambda N_Z(\lambda)} \tag{3.27}$$

where $Z_{in}(\lambda) = N_Z(\lambda)/D_Z(\lambda)$.

The order of $Z'_{in}(\lambda)$ should be one less than that of $Z_{in}(\lambda)$. However, as calculated in (3.27), it is in fact one degree higher than $Z_{in}(\lambda)$, due to a common factor $1 - \lambda^2$ in the numerator and denominator, which is divided out.

After the n-1 unit elements have been extracted, the input impedance of the remaining network is of the form

$$Z_{in}(\lambda) = \begin{cases} L_t\lambda + R_l, & n \text{ odd.} \\ (C_t\lambda + G_l)^{-1}, & n \text{ even.} \end{cases} \qquad (3.28)$$

Because of the choice of the gain factor K in (3.14) implicit in the form of (3.21) and (3.25), $R_l = 1.0$ for all odd order filters using these approximations, and $G_l = 1.0$ for even-order filters designed to implement (3.15). This is because, for filters of these types, maximum power transfer occurs in the equivalent ladder structure at zero frequency. This implies that $R_l = R_s$, and R_s has already been implicitly set equal to unity in (3.20). For even-order filters designed to realise the transfer function of (3.15), the value of G_l should be [74]

$$G_l = (\epsilon + (1 + \epsilon^2)^{1/2})^{-2} \qquad (3.29)$$

Thus the synthesis has realised a cascade of n-1 unit elements Z_1 to Z_{n-1}, followed by a stub and a resistance. The values of the inductances and capacitances of the equivalent circuit of the switched- capacitor filter are

$$\begin{aligned} L_1 &= Z_1 \\ C_2 &= 1/Z_1 + 1/Z_2 \\ L_3 &= Z_2 + Z_3 \\ &\vdots \\ L_n &= Z_{n-1} + L_t \quad (\text{for odd } n) \\ \text{or} \quad C_n &= 1/Z_{n-1} + C_t \quad (\text{for even } n) \end{aligned} \qquad (3.30)$$

3.3.3: Obtaining Capacitor Values.

The value of the termination is identical to that calculated above for the auxiliary network. The above expressions for the ladder element values are based on the equivalences established by Scanlan [76] although, for the terminating branch of an even-order filter, the technique used to calculate C_n is marginally simpler to program than that implied in [76].

The final step in the design procedure is to obtain values for the capacitance ratios in the switched- capacitor circuit which realises the filter. This is done by comparing co-efficients between the filter sections (i.e. the damped discrete integrators and the lossless discrete integrators) and the corresponding immittances

in the equivalent ladder network.

The transfer function of the non-inverting damped integrator of Fig. 2.1 (assuming l.d.i. phasing) can be easily shown (using the principle of conservation of charge) to be:

$$H(z) = \frac{V_0(z)}{V_{in}(z)} = \frac{C_1/(C_2 + C_3)\ z^{-1/2}}{1 - C_2/(C_2 + C_3)\ z^{-1}} \tag{3.31}$$

where C_1 is the input capacitor,
C_2 is the feedback capacitor,
and C_3 is the damping capacitor.

Dividing the right-hand side of (3.31) by $z^{-1/2}$ in numerator and denominator, and using the identities

$$\gamma = \tfrac{1}{2}\ (z^{1/2} - z^{-1/2}) \tag{3.32}$$
$$\mu = \tfrac{1}{2}\ (z^{1/2} + z^{-1/2})$$

it follows that

$$H(z) = \frac{1}{L\ \gamma + R\mu} \tag{3.33}$$

where, arbitrarily setting $C_1 = 1.0$,

$$L = 2\ C_2 + C_3 \tag{3.34}$$
$$R = C_3$$

The same equivalence is also found for the inverting damped integrator, and for the lossless integrators, where $R = C_3 = 0$.

Thus each branch in the equivalent circuit can be replaced by a switched-capacitor filter section, with the capacitor ratios chosen to satisfy (3.34) (where L is the value of the inductor in a series branch, or the value of a

capacitor in a shunt branch, and where $R = R_S$ for the input branch, $R = 0$ for the internal branches, and $R = R_l$ (G_l) for then output branch of an odd (even) order ladder). The resulting switched- capacitor filter will then have the desired frequencyresponse, provided that the clock phases for each integrator are appropriately chosen so that lossless discrete operation is performed, as discussed earlier.

3.3.4: Verification of the Design.

To verify the design, the design software allows plots of the following features to be obtained.

1) Having obtained $S_{11}(\lambda)$ by factorising (3.25) or (3.21), the program calculates the expected response of the filter by evaluating $|S_{11}(j\Omega)|^2$, where $\Omega = \tan(\pi f/f_S)$, in the passband. Hence, a plot of the passband response (to within a constant representing the filter gain) is obtained using the formula

$$|H_{21}(f/f_S)|^2 = (1 + \Omega^2)\ (\ 1 - |S_{11}(j\Omega)|^2) \qquad (3.35)$$

The plot obtained can then be assessed to ascertain the accuracy with which $S_{11}(\lambda)$ has been obtained from $S_{11}(\lambda)S_{11}(-\lambda)$.

2) To assess the accuracy of the realised switched- capacitor filter, it is simulated in the time domain. This is done by implementing the difference equations describing the filter operation, for an impulse input. The resulting time domain output is transformed into the frequency domain using Fast Fourier Transform techniques, and its amplitude spectrum is then plotted. The plot produced obviously allows a qualitative assessment of the success of the synthesis procedure to be obtained.

3.4: Variations on the Method of Synthesis.

Alternative algorithms are possible in the synthesis of this class of filters. Most alternatives suggested to date have focussed on methods to synthesise the network, given that an expression for the input impedance of the auxiliary network has been obtained as in (3.26).

3.4.1: Ladder Decomposition.

3.4.1.1: Theoretical Considerations.

Scanlan has suggested unit element extraction as a means of synthesising the network, based on the equivalence established by him between element values in the auxiliary network, and a cascade of unit elements with one stub. A more direct approach has been suggested [164].

Consider a network of the form shown in Fig. 3.10. $Z_{in}(\lambda)$ is assumed to be realisable as a ladder structure of the same form as the auxiliary networks of Fig. 3.7(b) and Fig. 3.9(b). The values of L and C are required, such that the impedance $Z(\lambda)$ can be further decomposed, so as to obtain the required ladder structure.

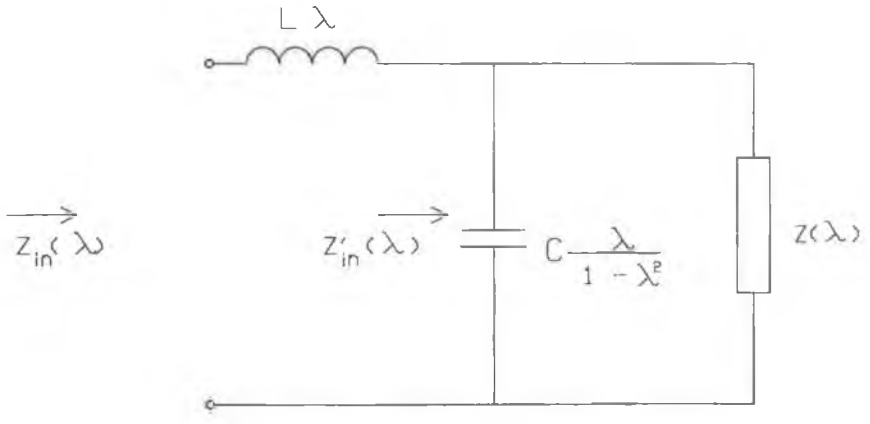


Fig. 3.10: Intermediate steps in the synthesis.

A value for L can be obtained by extracting the pole at infinity of $Z_{in}(\lambda)$.

$$L = \lim_{\lambda \to \infty} Z_{in}(\lambda)/\lambda \tag{3.36}$$

resulting in

$$Z'_{in}(\lambda) = Z_{in}(\lambda) - L\,\lambda \tag{3.37}$$

Then the value of C is calculated as

$$C = \lim_{\lambda \to 1} Y'_{in}(\lambda)\ (1-\lambda^2)/\lambda \tag{3.38}$$

This technique assumes the presence of a term $1-\lambda^2$ in the denominator of $Y'_{in}(\lambda)$, since otherwise $C \to 0$. In fact, the required root at $\lambda = 1$ does not exist. This problem arises because of the complete extraction of the pole at ∞ in (3.36). Instead, only a partial extraction of the pole at infinity should be attempted. The value of L should be chosen so as to ensure that $Z'_{in}(\lambda)$ has a pole at $\lambda = 1$. Evidently, the required value of L is given by

$$L = \lim_{\lambda \to 1} Z_{in}(\lambda)/\lambda \tag{3.39}$$

Now (3.38) will produce a non-zero result. After extracting the capacitor C, the value of the remaining impedance $Z(\lambda)$ is given by $1/Y(\lambda)$, where

$$Y(\lambda) = Y'_{in}(\lambda) - C\,\lambda/(1-\lambda^2) \tag{3.40}$$

This process is repeated until the remaining impedance (admittance) for an odd (even) order filter is of first order. This occurs after n-1 unit elements are extracted. For the odd order case, the impedance is then simply

$$Z(\lambda) = L\lambda + R_1 \tag{3.41}$$

For the even order case, the remaining admittance is

$$Y(\lambda) = (C\lambda + G_1)/(1 - \lambda^2) \tag{3.42}$$

which is the impedance of the parallel connection of a capacitor C, and, via a transformer of turns ratio $1:\mu^{1/2}$, a conductance G_1, as required at the output of Fig. 3.9(b). In both cases, the value of the load and the previous element can thus be easily obtained.

3.4.1.2: Practical Implementation.

The above extraction procedure has been incorporated into the synthesis program. In implementing the algorithm, care must be taken to eliminate all common factors of the form $1+\lambda$ or $1-\lambda$ from the numerator and denominator of the impedance function, so that the order of the impedance, as represented in computer memory, reflects the order of the corresponding circuit. This is done as follows, considering, for the purpose of exposition, a fifth order filter.

For such a filter, the input impedance will initially be of the form

$$Z_{in}(\lambda) = N_5(\lambda)/D_4(\lambda) \tag{3.43}$$

where the subscripts indicate the polynomial order. After partially extracting the pole at infinity, the impedance order is unaffected, since no degree reduction can result. However, a zero exists at $\lambda=1$, which has been deliberately introduced by the partial extraction process of (3.39), and a corresponding zero also exists at $\lambda = -1$, due to the nature of $Z_{in}(\lambda)$. Factoring out the resulting term of $1-\lambda^2$ yields

$$Y_{in}'(\lambda) = (1-\lambda^2)^{-1}\ N_4(\lambda)/D_3(\lambda) \tag{3.44}$$

Thus the value of C can be simply evaluated as

$$C = N_4(1)/D_3(1) \tag{3.45}$$

After extracting C, $Y(\lambda)$ is, from (3.40), of the form

$$\begin{aligned} Y(\lambda) &= (1-\lambda^2)^{-1}(\ N_4(\lambda)/D_3(\lambda) - C\lambda\ ) \\ &= (1-\lambda^2)^{-1}\ N_4'(\lambda)/D_3(\lambda) \end{aligned} \tag{3.46}$$

The numerator of $Y(\lambda)$ contains a term $1-\lambda^2$, which is factored out. Hence, the impedance, $Z(\lambda)$, remaining after the extraction of an inductor and a capacitor, is of the form

$$Z(\lambda) = N_3(\lambda)/D_2(\lambda) \tag{3.47}$$

Thus both numerator and denominator of the impedance have been reduced in degree by two. Clearly, degree reductions only occur after every second element has been extracted in this way.

The above description of the extraction process can be readily generalised for any order filter. After successively extracting an inductor followed by a capacitor, the impedance is finally reduced to the form $N_1(\lambda)/D_0(\lambda)$ for an odd-order filter, or $N_2(\lambda)/D_1(\lambda)$ for an even-order filter. Equations (3.41) and (3.42) respectively can then be used to complete the synthesis.

The parallels between the synthesis method described above and the technique of unit element extraction are evident. Both require impedances to be evaluated at $\lambda = 1$, and both feature factors of the form $1-\lambda^2$ (i.e. the terms realising the zeros in equation (3.9)). Thus, it is to be expected, *a priori*, that the numerical difficulties associated with both techniques are equivalent, and that no accuracy advantage will be present in one method over the other, making it more suitable for the synthesis of high order filters.

3.4.2: Use of General Synthesis Programs.

The above procedures for synthesis of the network require special programs for their implementation. An alternative procedure is suggested by the equivalent circuit used by Datar and Sedra [92] for the admittance $Y(\lambda) = C\lambda/(1-\lambda^2)$. They regard this as consisting of a capacitor of value C in series with an inductor of value -1/C, both of which vary with λ rather than the usual frequency variable 's'. Thus the admittance is $Y(\lambda) = 1/[(C\lambda)^{-1}-C^{-1}\lambda]$ which is of the required form.

It follows that, if a sufficiently general synthesis program is available, i.e. one that allows negative element values and real-axis transmission zeros, it can be applied to the synthesis of the network. A potential problem with this approach occurs with the load termination of even order filters, which will be resolved into a conductance G_l in series with an admittance $-G_l/\lambda^2$. This admittance is not in the form of any standard element (although it can be regarded as the dual of the frequency dependent negative resistor sometimes used in the design of active-RC filters). Thus, a general synthesis program may not be successfully applied to the

even order case.

3.4.3: Synthesis using the Transmission Matrix.

3.4.3.1: A formula for the Input Impedance.

The two techniques described above for obtaining a network realisation from the input impedance of the auxiliary network are general methods, applied to a specific synthesis problem. However, in [87], a new technique was presented, expressly for the synthesis of switched- capacitor ladder filters. The basis of this method is outlined below.

The input impedance of the auxiliary network, Z'_{in}, is obtained as before. Since the auxiliary network is obtained by impedance scaling the equivalent circuit of the switched- capacitor filter by $1/\mu$, it follows that the input impedance of the equivalent circuit is $Z_{in} = \mu Z'_{in}$. Note that this expression does not contain the input termination μR_S. It is the input impedance of an all-pole LC ladder (with frequency variable γ insteads of 's') terminated in a frequency variable resistor of value μR_1 (for an odd order filter) or $1/(\mu G_1)$ (for an even order filter).

The form of the transmission matrix for such a ladder structure may readily be determined, by, for example, finding the product of the transmission matrices of the ladder branches. For a filter of order n, it is of the form

$$\begin{vmatrix} A_{n-1}(\gamma) & B_n(\gamma) \\ C_{n-2}(\gamma) & D_{n-1}(\gamma) \end{vmatrix} \quad \text{(n odd)}$$

$$\begin{vmatrix} A_n(\gamma) & B_{n-1}(\gamma) \\ C_{n-1}(\gamma) & D_{n-2}(\gamma) \end{vmatrix} \quad \text{(n even)}$$

where the matrix entries are polynomials in γ whose order is indicated by the corresponding subscripts. The polynomials of odd order are odd functions of γ. Similarly, the even polynomials are even functions of γ, and equal unity when evaluated at $\gamma = 0$.

Thus the input impedance of the equivalent circuit is of the following

form:

$$Z_{in}(\gamma) = \frac{\mu R_1 \, A_{n-1}(\gamma) + B_n(\gamma)}{\mu R_1 \, C_{n-2}(\gamma) + D_{n-1}(\gamma)} \qquad (n \text{ odd})$$

$$= \frac{A_n(\gamma) + \mu G_1 \, B_{n-1}(\gamma)}{C_{n-1}(\gamma) + \mu G_1 \, D_{n-2}(\gamma)} \qquad (n \text{ even}) \tag{3.48}$$

If the expression for $Z_{in}(\gamma)$ can be put into the above form, then it immediately follows that the transmission matrix parameters are known. Since these are purely a function of γ, the ladder can readily be synthesised.

3.4.3.2: Evaluating the Transmission Matrix.

In [87], formulae are presented for the co-efficients of the transmission matrix parameters in (3.48) as a function of the co-efficients q_i, p_i of the auxiliary network input impedance,

$$Z_{in}(\lambda) = \frac{\sum_{0}^{n} q_i \, \lambda^i}{\sum_{0}^{n} p_i \, \lambda^i} \tag{3.49}$$

In the expression for (3.48) presented there, the values of R_1 and G_1 have been absorbed as scaling constants in $A(\gamma)$, $C(\gamma)$ (for odd-order filters) and in $B(\gamma)$, $D(\gamma)$ (for even orders). The values of R_1 and G_1 can be recovered easily from the formulae in [87] as $R_1 = A_{n-1}(0)$ for n odd, and $G_1 = D_{n-2}(0)$ for n even, since, in (3.48), the corresponding polynomials evaluate to unity at zero frequency.

The method used to obtain the transmission matrix parameters was not presented in detail in [87]. An outline of the method used for the odd case is presented below.

The identities

$$\lambda\mu = \gamma \tag{3.50}$$

and

$$\mu^2 = 1 + \gamma^2 \tag{3.51}$$

are used.

First the input impedance of the auxiliary network is written in the form

$$Z_{in}(\lambda) = \frac{E_n(\lambda^2) + \lambda\, O_n(\lambda^2)}{E_d(\lambda^2) + \lambda\, O_d(\lambda^2)} \tag{3.52}$$

where $E_n(x)$, $E_d(x)$ and $O_n(x)$ are polynomials in x of order (n-1)/2, and $O_d(x)$ is a polynomial of order (n-3)/2. Making the substitution

$$\lambda^2 \rightarrow \gamma^2/(1 + \gamma^2)$$

and multiplying the numerator and denominator of (3.52) by $(1+\gamma^2)^{(n-1)/2}$ results in the expression

$$Z_{in}(\lambda) = \frac{E_n'(\gamma^2) + \lambda\, O_n'(\gamma^2)}{E_d'(\gamma^2) + \lambda\, (1+\gamma^2) O_d'(\gamma^2)} \tag{3.53}$$

where $E_n'(\gamma^2)$ is an n-th order polynomial in γ^2 whose co-efficients are those of the numerator of $E_n(\lambda^2)$ when expressed as a function of γ^2, and where the other entries in (3.53) are similarly obtained.

$Z_{in}(\lambda)$ is now multiplied by μ to obtain $Z_{in}(\gamma)$, the input impedance of the equivalent circuit. It is observed that the resulting factor $\mu\lambda$ in front of $O_n'(\gamma^2)$ equals γ, and that the factor $\lambda\ (1+\gamma^2)$ in (3.53) can be written

$$(1+\gamma^2)\ \lambda = \mu^2\ \lambda = \mu(\mu\lambda) = \mu\gamma.$$

Comparing terms between the resulting expression for $Z_{in}(\gamma)$ and that given in (3.48) yields the result

$$\begin{aligned} A_{n-1}(\gamma^2)\ R_1 &= E_n'(\gamma^2) \\ B_n(\gamma^2) &= \gamma\, O_n'(\gamma^2) \\ C_{n-2}(\gamma^2)\ R_1 &= \gamma\, O_d'(\gamma^2) \\ D_{n-1}(\gamma^2) &= E_d'(\gamma^2) \end{aligned} \qquad (3.54)$$

Expanding out these expressions using the binomial theorem produces the expressions listed in [87]. A similar procedure produces the expression for the input impedance of the even order filter.

3.4.3.3: Synthesis.

The filter can now be synthesised as follows. Terminating the filter in a resistor of value R_1 instead of μR_1 results in an expression for $Z_{In}(\gamma)$ given by (3.48), but with μ set to unity. The ladder can then be synthesised using a continued fraction expansion around $\gamma = \infty$, and the resulting inductor and capacitor values are the same as those in the equivalent circuit of the switched- capacitor filter, which has the same transmission matrix parameters as the filter synthesised, although it is terminated in a frequency variable resistance, rather than a constant load. Hence the capacitance ratios required inthe switched- capacitor filter implementation can be obtained, using (3.34).

The above technique has been incorporated into the synthesis package, allowing its accuracy to be compared to that obtainable with the methods described earlier.

3.5: Other Techniques for Synthesis of l.d.i.-based Ladders.

Alternative solutions to the synthesis problem for l.d.i. ladders have been discussed in Chapter Two. Here further details will be briefly given on two of them.

3.5.1: The Datar-Sedra Approach [92]:

To differentiate their results from those of Scanlan [76], Datar and Sedra have applied his technique to a modified switched- capacitor ladder structure. The modification consists of including both an inverting and a non-inverting input (with nominally equal gains) in the first integrator of the circuit, for reading the filter input signal. Provided that the input signal is held on the appropriate phase (which may require the addition of another op-amp) this results in a filter transfer function (for odd-order filters) of μH_{21}, where H_{21} is the transfer function obtained using the same circuit, but with a conventional input stage, as treated by Scanlan. It follows that the resulting filter implements the same transfer function as the auxiliary network in [76] and so the approximation problem to be solved differs slightly from that discussed earlier. No formal solution to the approximation problem is presented, but a λ-plane function is given as an example for the maximally flat approximation. This corresponds to an amplitude response of

$$|H_{21}(\theta)|^2 = K/(1 + G_n^2(\sin(\theta)) \tag{3.55}$$

where $G_n(x)$ is given by

$$G_n(\sin(\theta)) = \left|\frac{\sin(\theta)}{\sin(\theta_0)}\right|^{n-1}\left|\frac{\tan(\theta)}{\tan(\theta_0)}\right| \tag{3.56}$$

where $\theta_0 = \pi f_0/f_s$, f_0 being the desired filter (3-dB) cutoff frequency, and f_s the sampling rate, although the constant given in (3.56) for specifying the required cutoff is not given in [92]. This approximation is known to be that required to achieve a maximally flat response around $\lambda = 0$ for a commensurate distributed filter consisting of n-1 unit elements and a stub [74]. The implication in [92] is that a new approximation problem is being solved, whereas solutions are already available to this problem.

The filter topology investigated in [92] has improved stopband selectivity compared with the conventional ladder because of the presence of a transmission zero at $\lambda = \infty$ (i.e. at $f = f_s/2$). However, it can only be applied to the design of odd order filters.

Datar and Sedra have also considered the case of the conventional switched- capacitor ladder, where their results, although couched in different

notation, are identical to those obtained earlier [76].

3.5.2: The Vaughan-Pope/Bruton Method [84]:

The technique proposed by the above authors was originally intended for use with digital filters, and their presentation uses the z-transform variable exclusively to represent signals in the frequency domain. However, when their results are transformed into the notation of [76], the similarity between the results of [76] and [84] become apparent. The technique in [84] was intended to be quite general, and used the concept of the two-pair network. Thus, in comparing the results of [84] and [76], the chain matrix of the appropriate two-port network must be derived from that of the two-pair network presented in [84]. The technique was applied to l.d.i.-based filters as an example. The method, when applied to such filters, may be described as follows, for odd-order filters, where $R_S = R_1$:

The transfer function to be implemented is of the form $-H^{-1}(z)$, which is equivalent to $H_{21}(\gamma)$.

The expression

$$K(z)K(z^{-1}) = H(z)H(z^{-1}) - 4\,\mu^2 \tag{3.57}$$

is evaluated, and the zeros inside the unit circle in the z-domain are assigned to K(z). The network is regarded as having terminations of the form $z^{-1/2}$ in which case the transmission matrix parameters A, B, C and D are related to H(z) and F(z) by

$$\begin{aligned} H(z) &= E(z) - z^{-1/2} F(z) \\ K(z) &= E(z) + z^{1/2} F(z) \end{aligned} \tag{3.58}$$

where

$$\begin{aligned} E(z) &= -B(z) - z^{-1/2} A(z) \\ F(z) &= D(z) + z^{-1/2} C(z). \end{aligned} \tag{3.59}$$

Hence the transmission matrix parameters can be obtained, and are found to be polynomials in γ.

The network is then synthesised by forming the input impedance with the output port open-circuited (thereby bypassing the problem of the frequency variable termination) and employing a continued fraction expansion about $\gamma = \infty$.

Manipulation of the formulae presented in [84] indicates that K(z) is, at least to within a scaling constant, equivalent to the expression S_{11}/H_{21} as those parameters are defined in [76,84], i.e.

$$K(z) = k\, S_{11}/H_{21} \tag{3.60}$$

where $|k| = 1$. It is thus equivalent to the so-called characteristic function used by some authors in the synthesis of doubly-terminated reactance two-ports [165] and so (3.57) can be regarded as a generalisation of Feldtkeller's equation:

$$|H|^2 = |K|^2 + 1 \tag{3.61}$$

which, in s-parameter notation, is usually written

$$|S_{11}|^2 + |S_{21}|^2 = 1 \tag{3.62}$$

In the Scanlan method, $|S_{21}|^2 = 4|\mu\, H_{21}|^2$. From (3.60)

$$|S_{11}|^2 = k^{-2}|K\, H_{21}|^2 = |K|^2\, |H_{21}|^2 \tag{3.63}$$

so (3.62) becomes

$$|K|^2 + 4\mu^2 = |H_{21}|^{-2} \tag{3.64}$$

or

$$K(z)K(z^{-1}) = H(z)H(z^{-1}) - 4\,\mu^2 \tag{3.65}$$

Thus the method of obtaining K(z) in [84] is essentially equivalent to that used in [76] to obtain $S_{11}(\lambda)$. It is thus expected that the numerical problems encountered with both will be similar, although it is anticipated, *a priori*, that operating in the z-plane increases the severity of the numerical problems encountered.

The technique of [84] has been redescribed recently in [86]. There a method of approximation which achieves an equiripple pass-band is described. The method used is lengthy and involved, and results in a cumbersome expression for $|H_{21}|^2$. This derivation is in fact unnecessary, since the optimal solution to this approximation problem has long been available [76,82].

3.6: Results Obtained.

The synthesis program developed can synthesise all-pole filters of the type considered in [76] and incorporates the following features:

The low-pass filter approximation features either an equiripple passband, or a maximally flat response at d.c. Three of the synthesis methods described earlier are supported, namely:

1) The original technique of [76], using unit element extraction (described in (3.3.2)).

2) The technique of [76], modified to perform a ladder decomposition on the auxiliary network (described in (3.4.1)).

3) The synthesis technique of [87] (described in (3.4.3)).

It has been found that all the techniques work well for filters up to about sixth order. Thereafter, the third technique proves to be superior, producing accurate results for filter orders up to 12-16, the exact order achievable depending on the cutoff frequency and (for equiripple pass-band filters) ripple specifications chosen, while the other techniques invariably fail for filter orders higher than eight.

As an example, a filter with the following specifications is considered:

Approximation type:	equiripple pass-band.
Passband Ripple:	0.5 dB.
Cutoff Frequency:	$f_S/16$.
Filter Order :	8,9,12.

Considering first the eighth-order filter, the expected passband response, as determined using (3.35), is shown in Fig. 3.11. The plot obtained is based on the response calculated at sixty four evenly spaced frequencies in the passband. The response obtained at each point is marked by a cross in Fig. 3.11, and the plotting routine joins the points by straight lines to approximate a continuous curve. The points plotted are, to a very high accuracy, in the positions expected from (3.16), indicating that $S_{11}(\lambda)$ has been obtained correctly. (The apparent droop in the passband response around $f/f_S = 0.06$ occurs because only a few points are plotted there - there are numerical difficulties associated with calculating (3.35) at closer frequency intervals in this region.)

Table 3.5 shows the element values obtained for the equivalent circuit of Fig. 3.9(a) for the three synthesis methods considered. The pass-band response obtained by simulating the three filters in Table 3.5 are shown in Figs. 3.12, 3.13 and 3.14 for the first, second and third methods. Clearly the passband responses for the first and second methods are not equiripple, that in Fig. 3.12 deviating most from that intended (i.e. Fig. 3.11). In contrast, the correspondence between Figs. 3.11 and 3.14 is excellent.

The corresponding element values for a ninth-order filter are shown in Table 3.6. Again, $S_{11}(\lambda)$ has been obtained accurately, as demonstrated by Fig. 3.15. The value of the last inductor for the first two methods is negative, indicating that these methods have failed to synthesise the filter correctly. In fact, the element values for the second method result in an unstable filter, so no plot of passband response can be obtained. The time domain simulation of the filter synthesised using the second method, when transformed into the frequency domain using the FFT, results in the pass-band response of Fig. 3.16, which is clearly incorrect. Once again, the results obtained by the third method are excellent, as shown in Fig. 3.17.

The superiority of the method of [87] is thus demonstrated. Using the values obtained by this method as a reference, it can be seen that, for the other two methods, the values of the extracted elements diverge appreciably from the correct values after five elements have been extracted. Improvements in the numerical techniques used might improve this figure (e.g. both methods return an incorrect value for the load termination, which can be calculated before commencing the synthesis as $Z_{in}(\lambda=0)$, and this error might be corrected for).

However, the third method is far superior, as demonstrated by its success in synthesising a twelfth order filter, whose element values are listed in Table 3.7. The response required of this filter, as determined from (3.35), is shown in Fig. 3.18, and the response obtained, shown in Fig. 3.19, is in excellent agreement.

Fig. 3.18 , bearing in mind the resolution limitations of the obtained plot, can be shown to be the required equiripple-passband amplitude response, indicating that $S_{11}(\lambda)$ has been obtained accurately for the twelfth-order design.

	Element values		
	Method 1	Method 2	Method 3
R_S	1.000	1.000	1.000
L_1	10.56	10.56	10.56
C_2	6.315	6.315	6.315
L_3	14.06	14.06	14.05
C_4	6.798	6.798	6.798
L_5	14.14	14.14	14.14
C_6	6.593	6.593	6.591
L_7	13.11	13.11	13.25
C_8	4.460	3.954	3.896
G_1	0.578	0.522	0.504

Table 3.5: Element values for the eighth-order filter.

	Element values		
	Method 1	Method 2	Method 3
R_S	1.000	1.000	1.000
L_1	10.53	10.53	10.53
C_2	6.398	6.398	6.398
L_3	13.93	13.93	13.93
C_4	6.990	6.990	6.990
L_5	13.90	13.90	13.90
C_6	6.969	6.967	7.060
L_7	61.88	66.35	13.25
C_8	0.01659	.01038	6.661
L_9	-418.8	-48.79	7.788
R_1	1.000	1.000	1.000

Table 3.6: Element values for the ninth-order filter.

	Element values		
	Method 1	Method 2	Method 3
R_S	—	—	1.000
L_1	—	—	10.63
C_2	—	—	6.397
L_3	—	—	14.19
C_4	—	—	6.954
L_5	—	—	14.38
C_6	—	—	7.021
L_7	—	—	14.38
C_8	—	—	6.966
L_9	—	—	14.26
C_{10}	—	—	6.670
L_{11}	—	—	13.33
C_{12}	—	—	3.931
G_1	—	—	0.504

Table 3.7: Element values for the twelfth-order filter.

The synthesis technique of [84] has not been programmed. The analysis

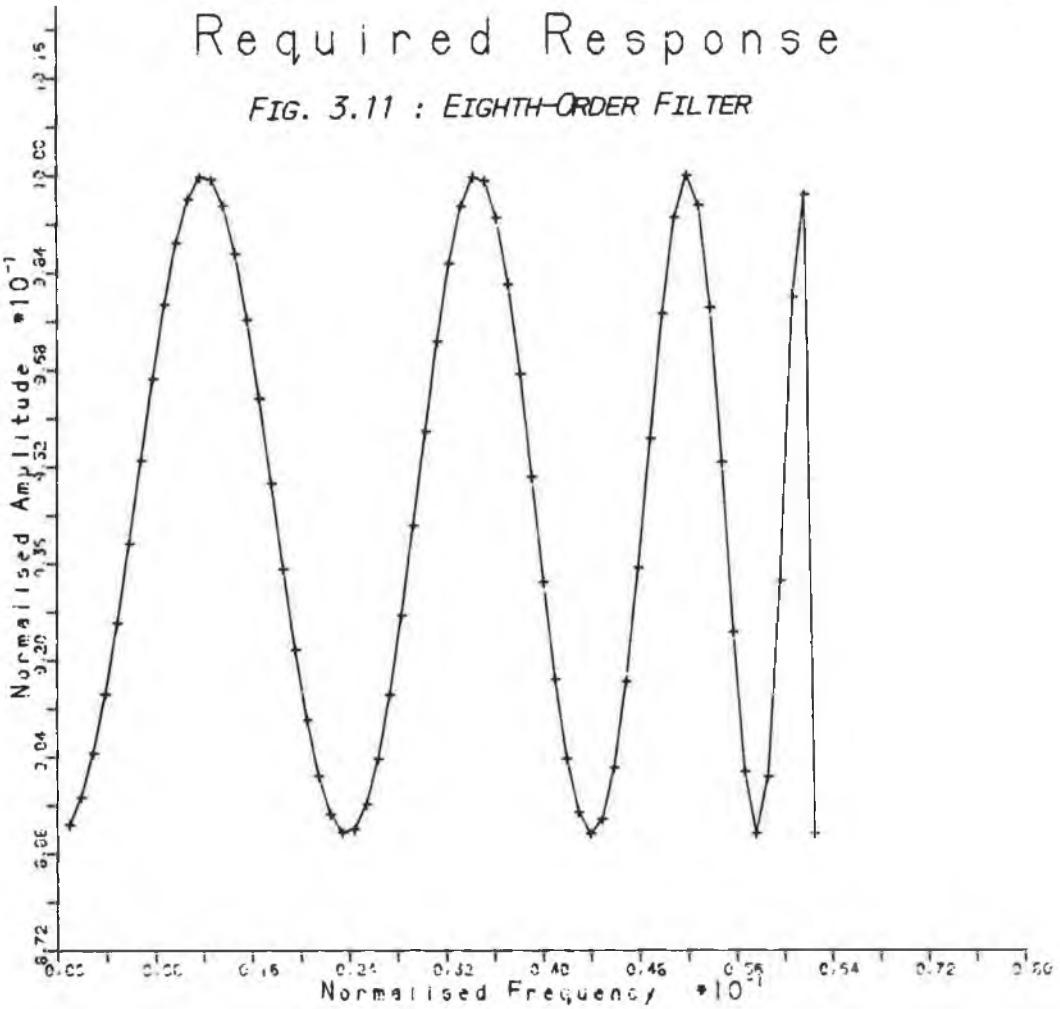


FIG. 3.11 : EIGHTH-ORDER FILTER

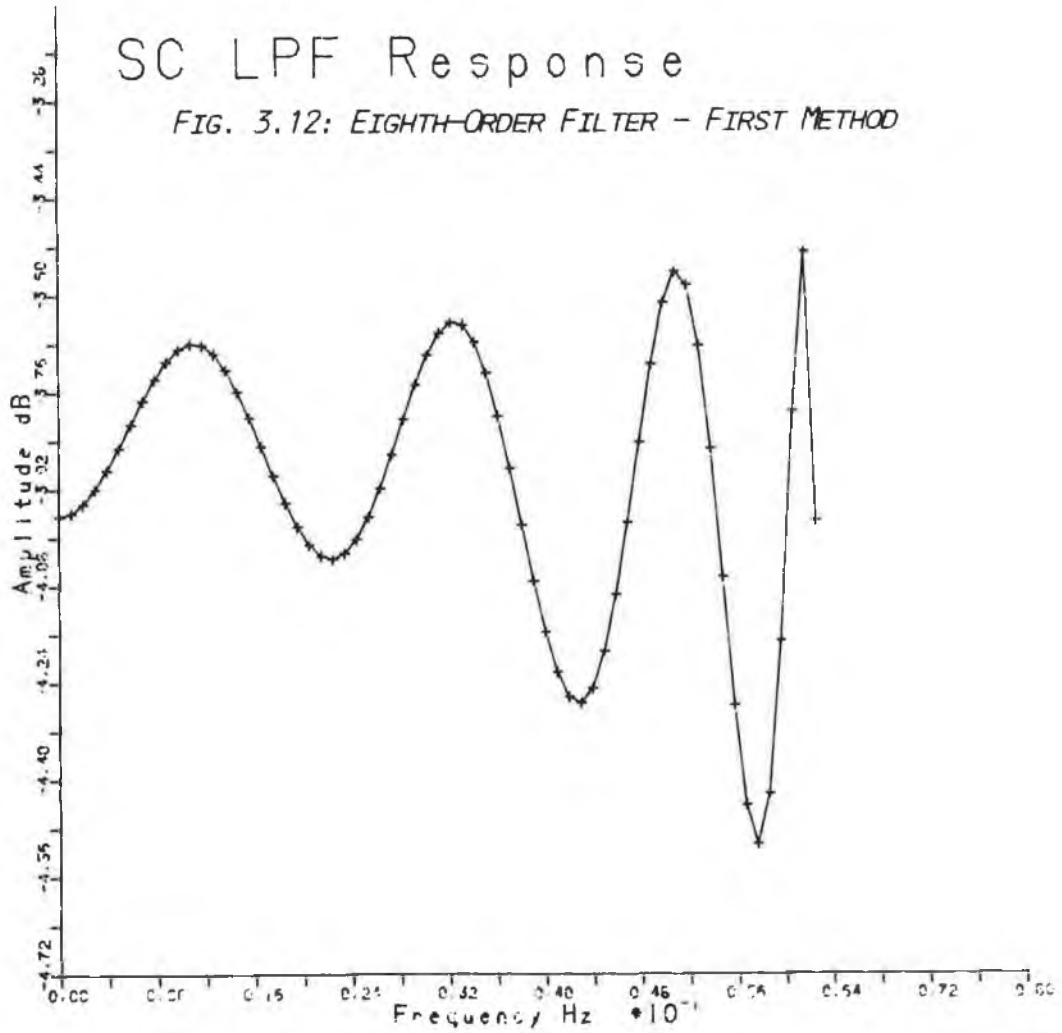


FIG. 3.12: EIGHTH-ORDER FILTER - FIRST METHOD

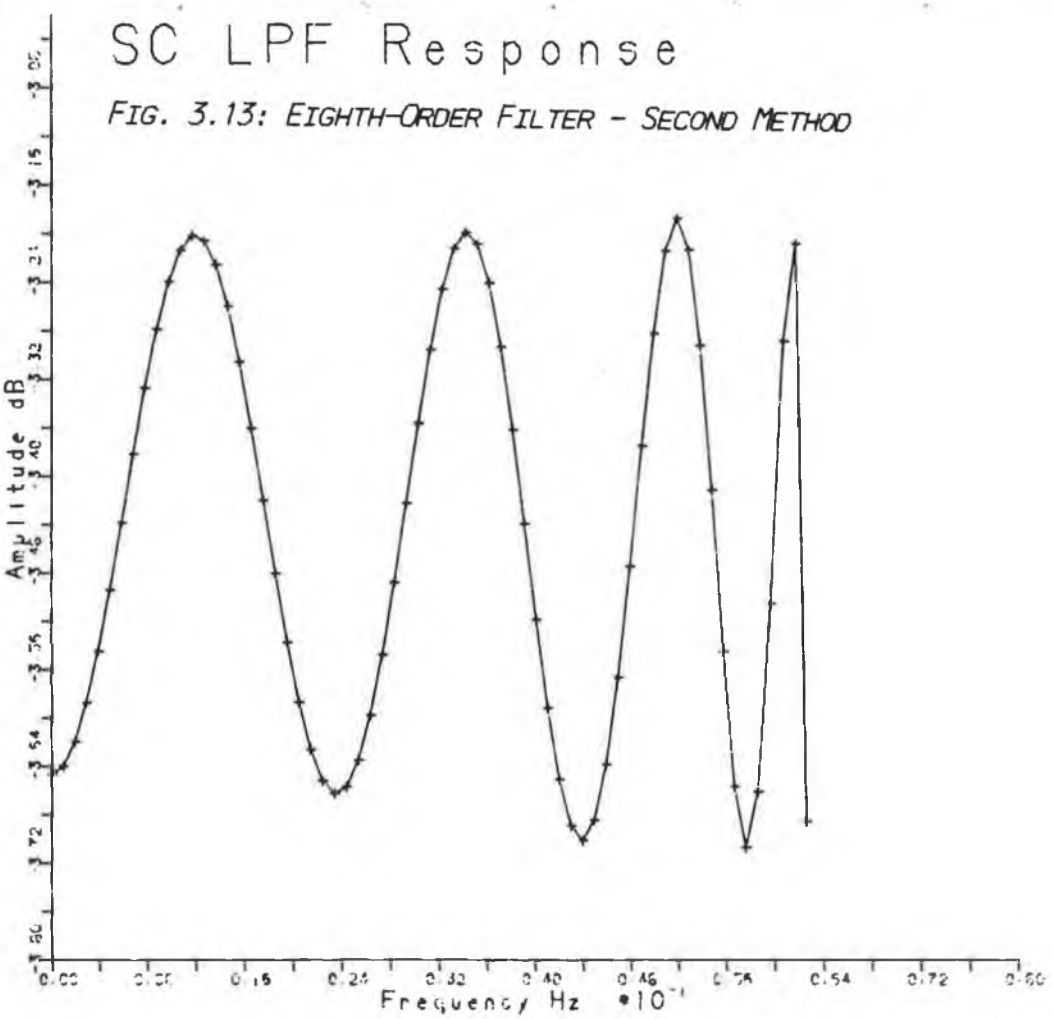


FIG. 3.13: EIGHTH-ORDER FILTER - SECOND METHOD

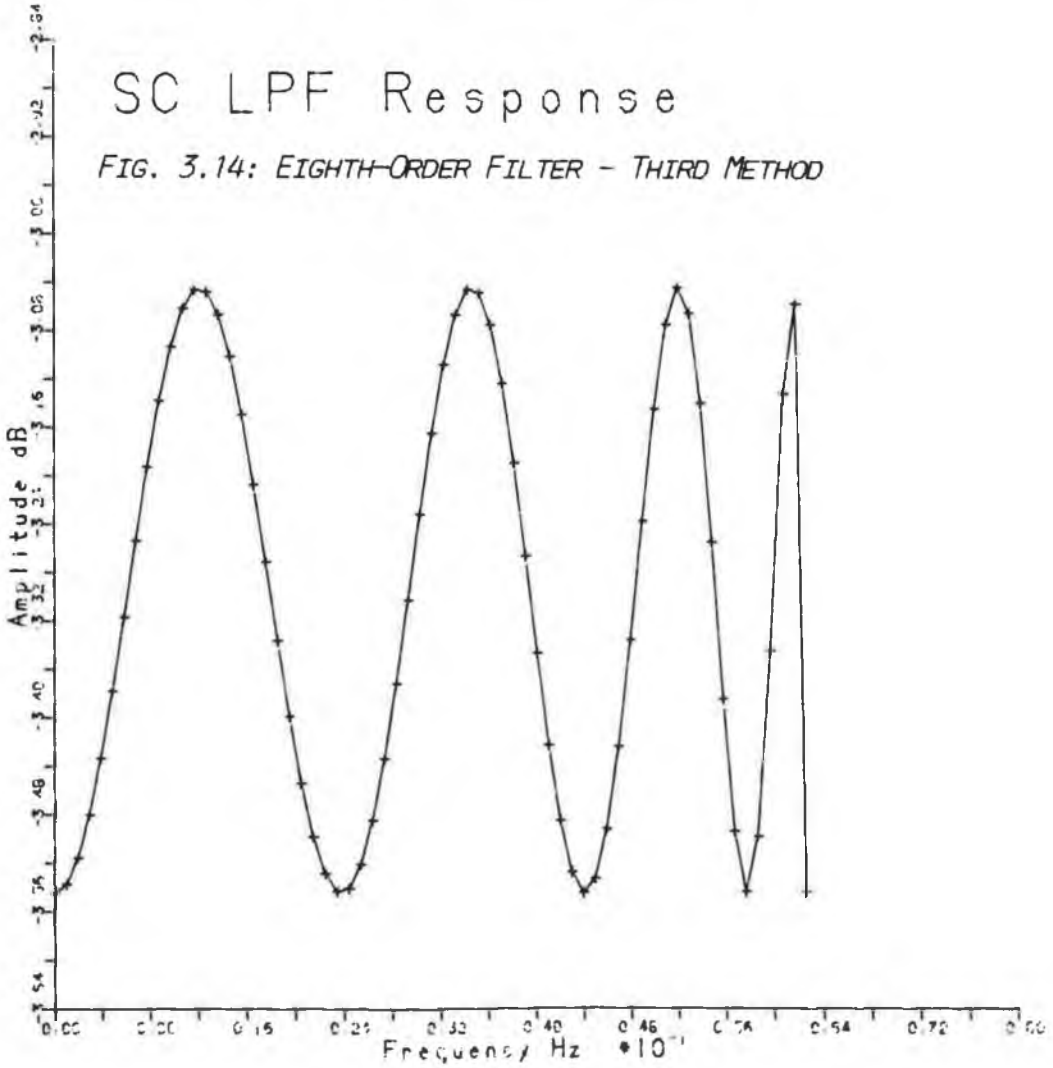


FIG. 3.14: EIGHTH-ORDER FILTER - THIRD METHOD

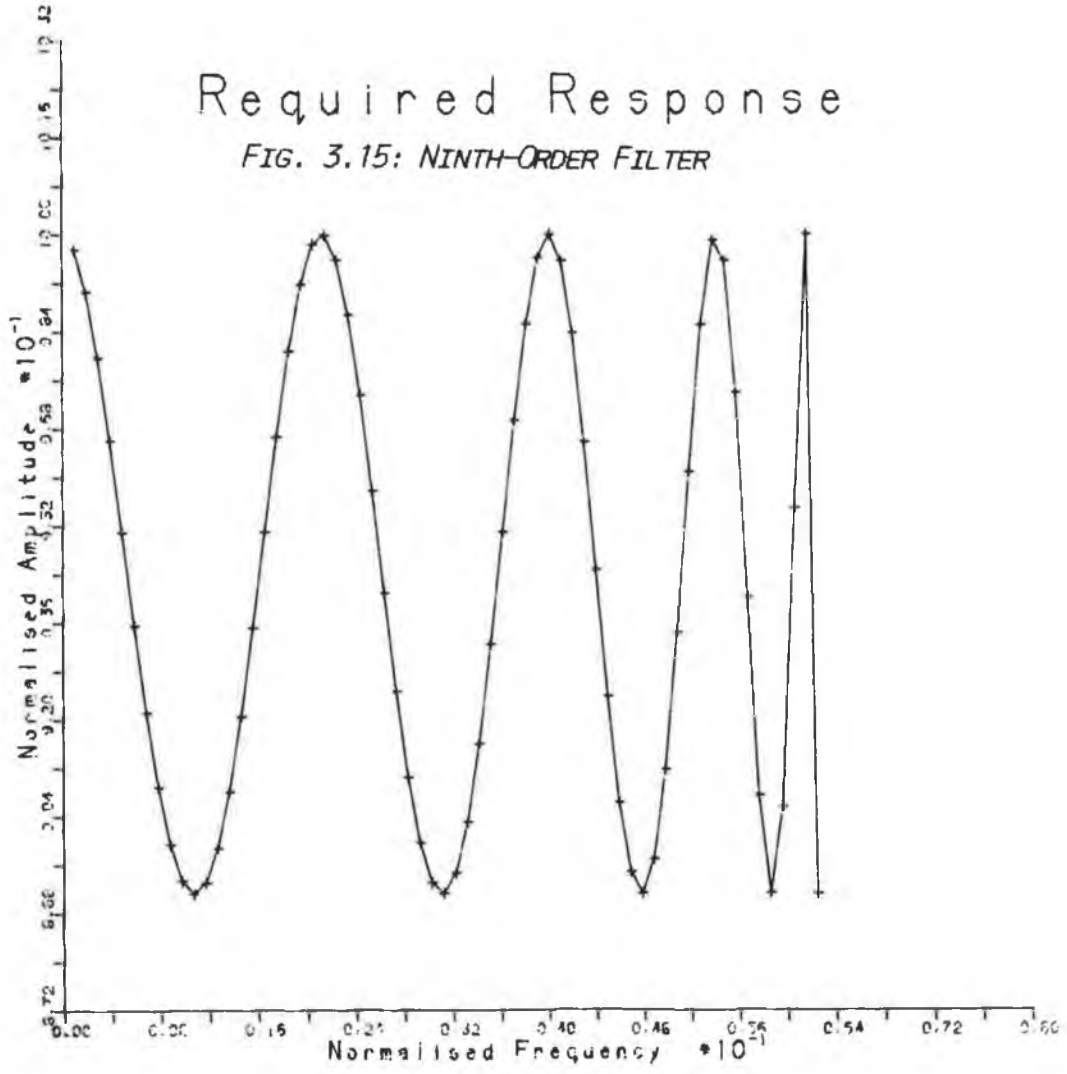


FIG. 3.15: NINTH-ORDER FILTER

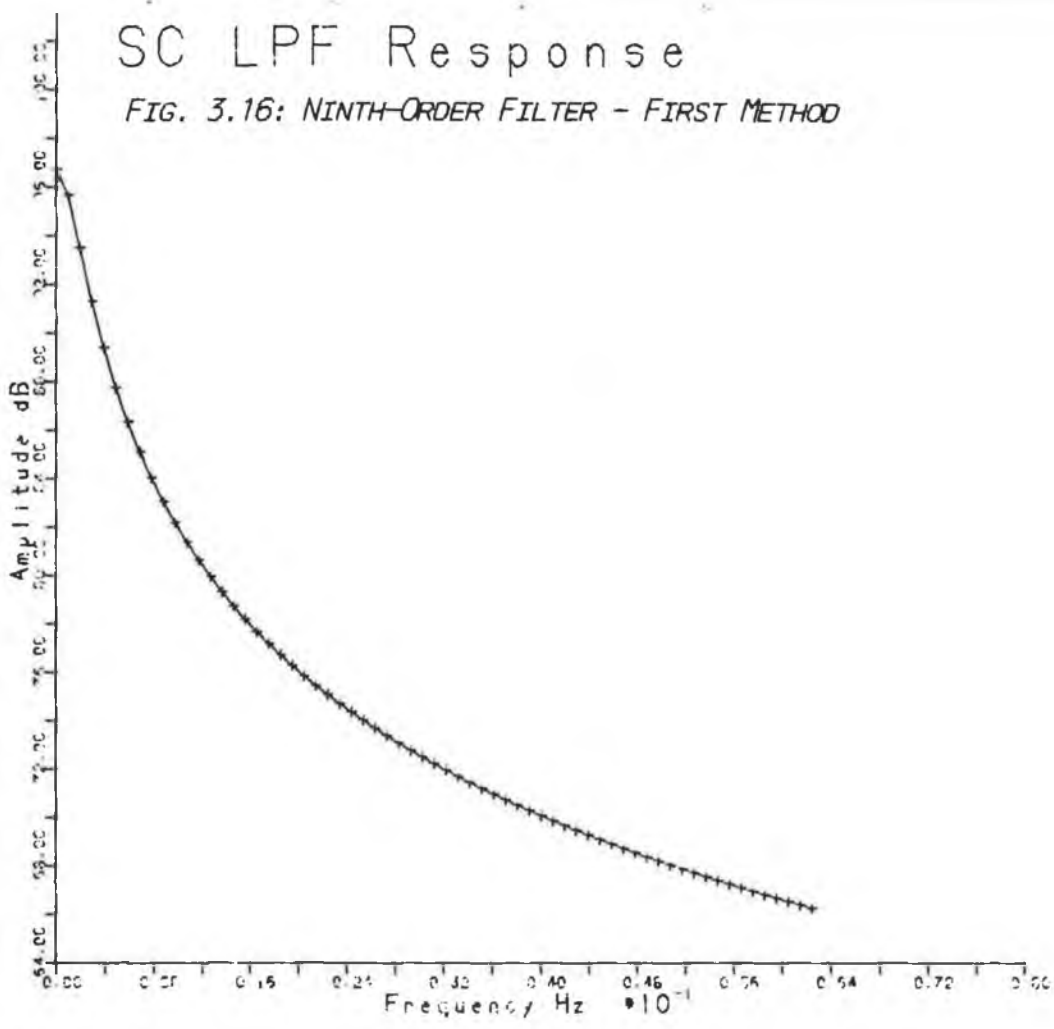


FIG. 3.16: NINTH-ORDER FILTER - FIRST METHOD

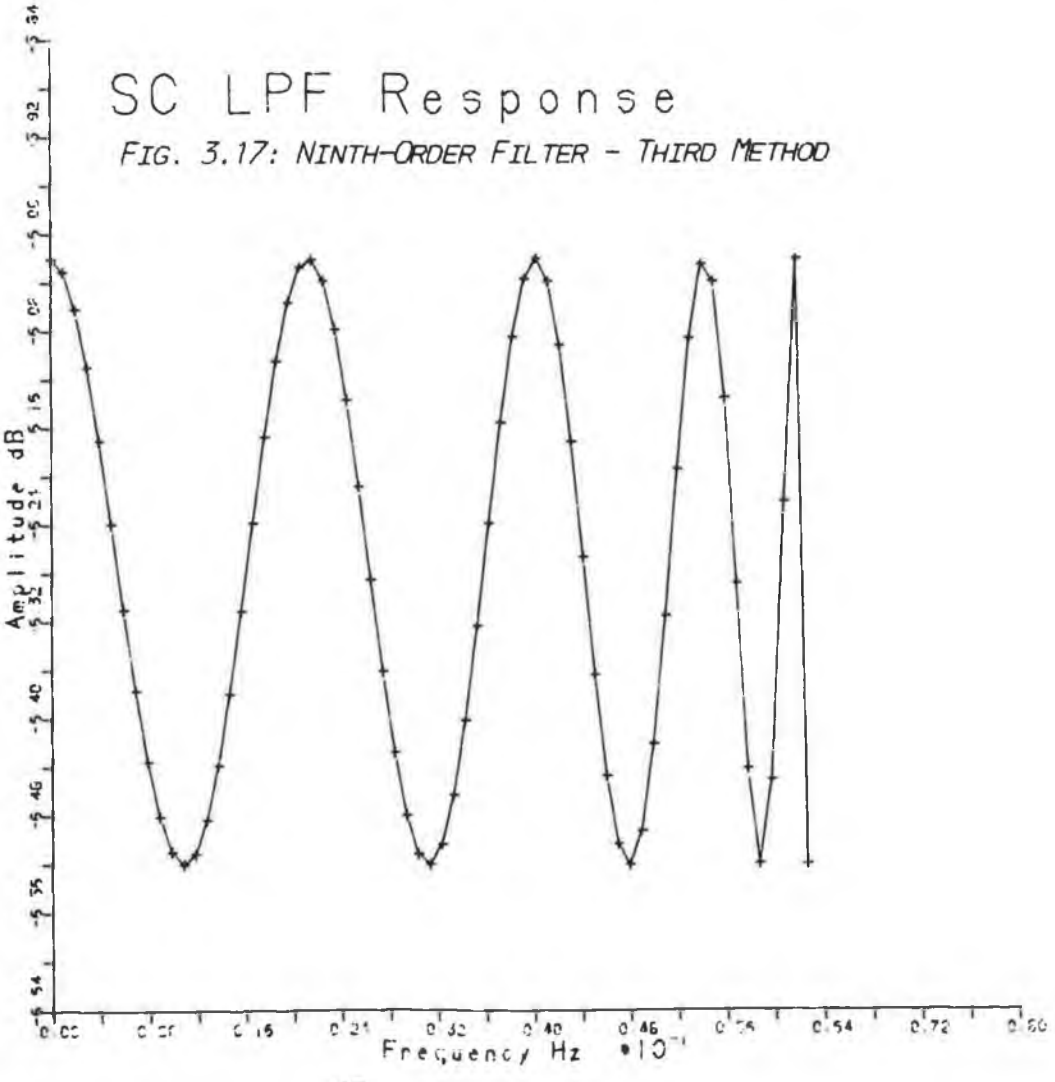


FIG. 3.17: NINTH-ORDER FILTER - THIRD METHOD

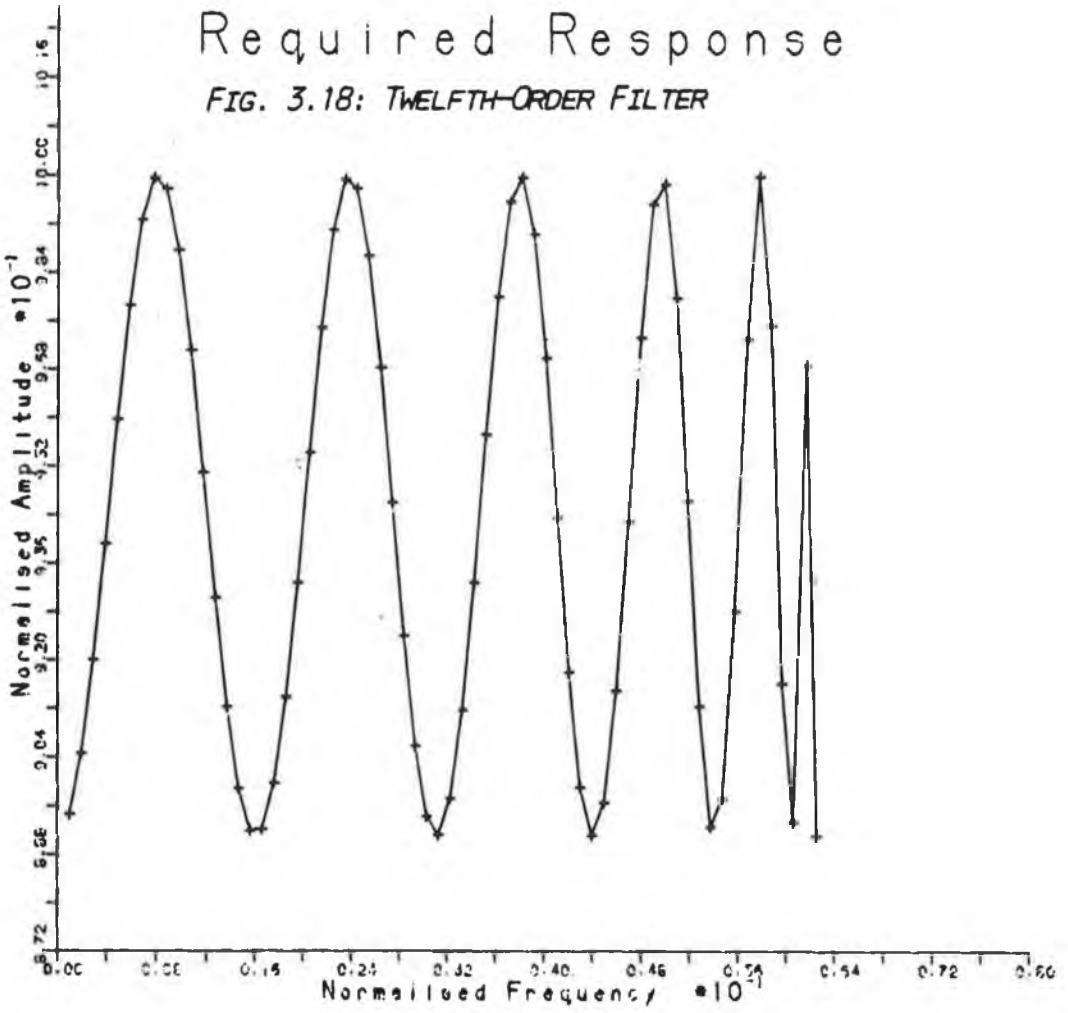


FIG. 3.18: TWELFTH-ORDER FILTER

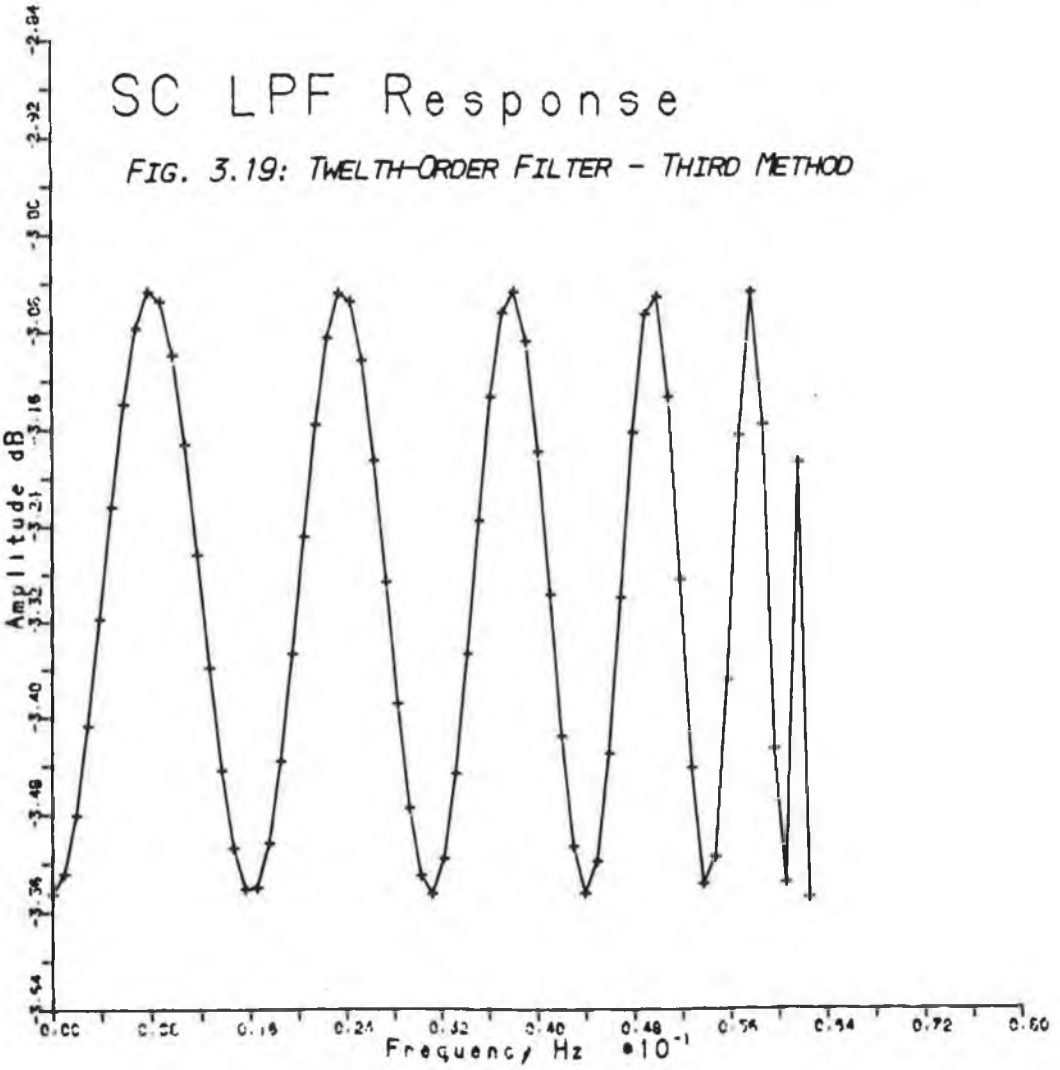


FIG. 3.19: TWELTH-ORDER FILTER - THIRD METHOD

given earlier indicates that the results obtained are expected to be broadly similar to those obtainable with the Scanlan technique, although finding the characteristic equation in the z-plane may produce less accurate results than performing the synthesis in the λ-plane. A FORTRAN program has already been published which implements the Vaughan-Pope/Bruton algorithm [86]. Satisfactory results are not obtained for filter orders greater than ten, in spite of the use of special root-finding techniques for factoring $K(z)K(z^{-1})$, which the authors consider to be the main source of error. A constraint, based on some elementary numerical analysis, is presented which must be satisfied if the FORTRAN program is to synthesise an equiripple passband filter successfully, which is, for the particular implementation,

$$\epsilon^2 (4/(\pi f/f_s))^{2n} \leqslant 10^{12}, \qquad n<10.$$

3.7: Conclusions.

The main sources of inaccuracy in the design algorithm used to obtain the results presented above are:

1) The formulation of $S_{11}(\lambda)$ from $S_{11}(\lambda)S_{11}(-\lambda)$.

2) The technique used to extract element values from the calculated expression for Z_{in}.

The results obtained indicate that the second factor is most significant in limiting the order of filter which can be synthesised. In fact, analytical expressions can be obtained for the $S_{11}(\lambda)$ pole locations for the approximations used in (3.12)- (3.14). This is because the γ-plane poles of $S_{11}(\lambda)S_{11}(-\lambda)$ can be found from the pole locations for the corresponding LC ladder in the s-plane. For example, for an LC low-pass ladder, designed to provide an equiripple passband, and with the passband edge at $\omega = 1$, the poles occur at [74]

$$s_i = \pm(\eta \sin \alpha_i - j \sqrt{(1+\eta^2)} \cos \alpha_i), \quad i=1,..,n \tag{3.66}$$

where $\alpha_i = \frac{1}{2}\pi (2i-1)/n$ and $\eta = \sinh(n^{-1} \sinh^{-1}(\epsilon^{-1}))$. Suppose one such pole occurs at $s = s_j$, with $s_j=r+jx$, $r>0$, and $x>0$. Then, from (3.66), it follows that three other poles occur at $s = -s_j$, and $s = \pm s_j^*$.

The corresponding γ-plane poles of $S_{11}(\lambda)S_{11}(-\lambda)$ occur at

$$\gamma_i = \sin \theta_o \; s_i \tag{3.67}$$

This corresponds to a fourth order term in $S_{11}(\lambda)S_{11}(-\lambda)$ of the form $\gamma^4+b\gamma^2+c$. Substituting

$$\gamma^2 = -\lambda^2/(1-\lambda^2) \tag{3.68}$$

it follows that the corresponding λ-plane poles of $S_{11}(\lambda)$ are at

$$\lambda_j = \pm(2+2c)^{1/2} \; [2c+b \pm j(4c+4b-b^2)^{1/2}]^{1/2} \tag{3.69}$$

The two poles in the right-half λ-plane are assigned to $S_{11}(\lambda)$. For filters of odd order, one of the poles of $S_{11}(\lambda)$ is purely real. The procedure described above is appropriately modified to evaluate this pole.

The problem still remains of analytically determining the zeros of $S_{11}(\lambda)S_{11}(-\lambda)$, which are the solutions of the equation

$$N(\lambda)N(-\lambda) - 1 + \lambda^2 = 0 \tag{3.70}$$

where $N(\lambda)$ is the denominator of $S_{11}(\lambda)$. Thus, the accuracy with which the roots of (3.70) can be determined limits the achievable filter order. However, the results presented here indicate that, when performing the synthesis in the λ-plane, it is in the extraction of element values, after evaluating $S_{11}(\lambda)$, that appreciable error is introduced. This limitation may be overcome by the use of new or improved synthesis techniques.

Chapter Four : SENSITIVITY ANALYSIS OF SC FILTERS

4.1: Structures for Low Sensitivity Filters.

The switched- capacitor filters of the previous chapter feature a circuit operation which simulates that of a passive doubly-terminated lossless ladder. The motivation behind such a design is to reproduce the low passband sensitivity achievable by the passive filter.

A description of how a doubly terminated passive lossless ladder can feature low passband sensitivity was first given by Orchard [29]. His argument was based on the power transfer limitations of such a filter, and can be applied to any passive lossless structure, i.e. any filter which can be regarded as a reactance two-port between resistive terminations. Since such a filter is doubly terminated, there is a limit to the amount of power that can be supplied by the source. Since it is passive, the power delivered to the load cannot exceed that supplied by the source, and since it is lossless, the power in the load equals that supplied. The power flow is often regarded, by analogy with the physics of transmission-line systems, as follows.

The source is regarded as always supplying its maximum power P_{max} to the input port of the two-port. Part of that power is regarded as being reflected at the input port due to a mismatch (the input impedance of the two-port does not match the source resistance). Only the remaining power P_0 is transmitted through the two-port to be developed across the load termination. Using the notation of scattering parameters, it follows that P_0/P_{max} equals $|S_{21}|^2$, where S_{21} is the forward transmission co-efficient of the two-port, and $|S_{21}|^2$ is the transducer power gain [74]. It follows that the transducer power gain for such a filter satisfies the constraint

$$|S_{21}|^2 \leq 1. \tag{4.1}$$

Suppose that the filter is designed so as to attain maximum power transfer at some frequencies in the passband. For the typical case of an equiripple passband, these frequencies correspond to the ripple maxima. At such a frequency, say $f = f_1$,

$$|S_{21}|^2 = 1 \tag{4.2}$$

If any of the element values for the filter are now perturbed from their ideal values, the frequency response will change. The upper bound in (4.1) cannot be exceeded and so it follows that, if a graph is plotted of the transducer power gain at frequency f_1 against x, where x is the value of an element in the filter (typically an inductor or capacitor) whose value is x_{ideal} for the ideal filter, then the graph will have a maximum at x_{ideal} (assuming all other elements to have their ideal values) as shown in Fig. 4.1. In other words

$$\partial/\partial x(|S_{21}|^2) = 0 \tag{4.3}$$

when evaluated at $f = f_1$ for $x = x_{ideal}$.

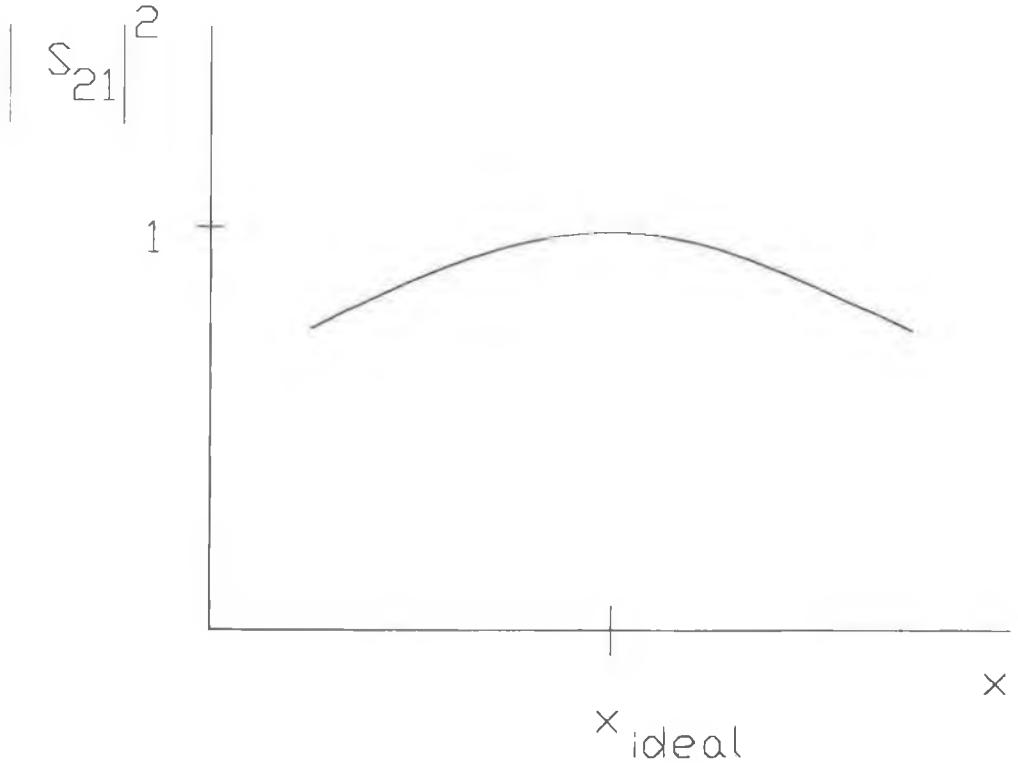


Fig. 4.1: Transducer power gain.

This means that the first order sensitivity of the filter amplitude response to variations in the value of x about its nominal value is zero at frequency f_1 (and at any other frequency where $|S_{21}|^2 = 1$).

Such a feature is very attractive in practical filters, since absolute precision is not available in realising the filter. Thus, in practice, where a filter is designed to have a transducer power gain of

$$F(\omega,\underline{x}) = |S_{21}|^2 \tag{4.4}$$

at frequency ω, where $\underline{x}$ is the vector of ideal element values, in fact the realised response is $F(\omega,\underline{x}+\Delta\underline{x})$ where $\Delta\underline{x}$ is the error in the realised element values. (To be completely general, some of the entries in $\underline{x}$ can have a nominal value of zero, the corresponding entries in $\Delta\underline{x}$ being the values of parasitics in the fabricated filter.)

Expanding the function F in a Taylor Series, and retaining only the first derivatives, results in the following approximation for the filter error

$$E(\omega,\Delta\underline{x}) = \Delta\underline{x}.[\partial/\partial\underline{x}\ F] \simeq F(\omega,\underline{x}+\Delta\underline{x}) - F(\omega,\underline{x}) \tag{4.5}$$

The first order sensitivity of a filter response F to variations in a parameter x is frequently defined as [166]

$$S^F_x = (x/F)\ \partial/\partial x(F) \tag{4.6}$$

When F is the amplitude-squared response $|H_{21}|^2$ of the filter, then this sensitivity expression is zero when maximum power transfer occurs, for the elements in the reactance two-port (which for an LC filter are the inductors and capacitors) although not for the terminations, because $|H_{21}|^2$ is a function of the terminations, as well as of the transducer power gain $|S_{21}|^2$. Thus the first order error defined in (4.5) is at a minimum at any point in the pass-band where maximum power transfer occurs.

Because of this property of doubly terminated passive lossless filters, they are often used as prototypes or models when active or digital filters are being designed, with the goal of retaining the property of low passband sensitivity. There is no guarantee that this property will be retained, since the operation of the new filter may not be directly analogous to that of the prototype [167], new sensitivities being introduced not present in the prototype.

It follows that, when a filter has been designed whose operation in some way simulates that of a passive filter with low passband sensitivity, the sensitivity of the new filter must be evaluated to see if this property has been preserved.

The argument above applies only to the passband sensitivity. Ladder filters are also known to possess good stopband sensitivity [165,168] unlike, for example, lattice filters, where the stopband loss is dependent on the balancing of impedances in the lattice arms, and which, in consequence, feature poor sensitivity in the stopband [165,168].

Consequently, doubly terminated passive ladder filters are frequently chosen as the prototype for active-RC, digital or switched- capacitor filter designs. A number of methods can be used to derive the new filter structure. The most direct, applicable to analog filters, is to replace the inductors in the prototype by op-amp sections which feature the same relationship between voltage and current, a technique known as inductor simulation. Another is to model the flow of wave signals through the prototype, and to use building blocks which reproduce that wave flow [168]. One of the most popular techniques is to regard the currents and voltages in the prototype as state variables, and to construct a filter whose state variables are governed by the same equations or, equivalently, which features the same signal flowgraph. Such a filter design is the 'leapfrog ladder' of Girling and Good [160]. The switched- capacitor filters of Chapter Three have been based on such a simulation of the low-pass ladder, and their sensitivities are now investigated.

4.2: Techniques for Sensitivity Analysis.

4.2.1: A Formula for Lossless Two-ports.

No simple analytical expressions are available for the sensitivity of ladder filters. Orchard, Temes and Cataltepe have recently obtained the following expression for the sensitivity of a doubly-terminated lossless two-port to variations in the value of an internal impedance z_i,

$$\frac{\partial \theta(j\omega)}{\partial z_i} = \frac{|I_i|^2 + S_{11}^*(j\omega) I_i^2(j\omega)}{2P_0} \tag{4.7}$$

where P_0 is the power delivered to the load termination, I_i is the current flowing through impedance z_i, and $\theta = -\ln S_{21}(j\omega)$ [169,170].

Using this formula, a single analysis of the network suffices at a given frequency for the sensitivities of the filter response to be evaluated. This analysis must determine the values of I_S (to find S_{11} and S_{21}), I_l (to find P_0 and S_{21}) and I_k, the current flowing through z_k. A dual version of (4.7) can be applied to evaluating the sensitivity to an admittance.

4.2.2: A Formula for Signal Flowgraphs.

Another technique for analytically determining the filter sensitivity can be applied to the signal flowgraph of the filter. Assume that the signal flowgraph is such that only one path from the signal flowgraph input node to the output node exists for which each branch in the path is traversed once only. The signal flowgraph of a filter of the type currently being discussed will be of this form. This path is known as the forward path. Denote the transmission of the i-th branch in the forward path by T_i. Then the gain in the forward path is $T = \prod T_i$. All other branches of the signal flowgraph are assumed to start and end at nodes on the forward path. Define the expression D as

$$D = T/F \tag{4.8}$$

where F is the overall transfer function for the signal flowgraph. Then it can

be shown that the sensitivity (as defined by (4.6)) of the filter transfer function to variations in the value of a branch transmittance is

$$S^{F}_{x} = D'/D - \epsilon \tag{4.9}$$

where D' equals the expression for D evaluated for $x = 0$, and where $\epsilon = 0$ if the branch is on the forward path, and $\epsilon = 1$ if the branch is a feedback branch [171].

This result can be easily verified. Using Mason's rule for the transfer function of a signal flowgraph, it can be shown that the function D is a linear function of the branch transmissions x, i.e.

$$\frac{\partial^2 D}{\partial x^2} = 0 \tag{4.10}$$

It follows that D can be expressed as

$$D = D_1(x) + D_2 \tag{4.11}$$

where the function D_2 is independent of x, and D_1 is a linear function of x (and of the other transmissions) which is zero for $x = 0$. Thus

$$\partial/\partial x(D) = D_1(x)/x = (D - D(x=0))/x \tag{4.12}$$

since $D_2 = D(x=0)$. Noting that $\partial/\partial x(T) = T/x$ for a branch on the forward path, and equals zero for a feedback branch, the result follows by a straightforward application of the quotient rule for partial derivatives.

This sensitivity formula is simple, and is easy to apply when an analytical expression is required. When numerical results are required however, it poses difficulties, since the values of D and D' are not easily evaluated by computer.

4.2.3: A Formula which Employs Transposed Signal Flowgraphs.

An alternative technique for sensitivity analysis is the use of the adjoint network, in an application of Tellegen's Theorem [165]. This technique has been generalised to cover any network described by a signal flowgraph [172]. (Tellegen's theorem, in the original form, is derived from Kirchoff's laws and so is not directly applicable to, for example, sampled-data filters.) This latter technique is most appropriate for calculating the sensitivities of switched- capacitor filters of the type in the previous chapter, which are based on the signal flowgraph simulation of ladder filters, and potentially offers more flexibility than, for example, the technique suggested by (4.7), in that the filter signal flowgraph is not constrained to be equivalent to that of a passive structure, so that departures from exact ladder simulation in the realised filter can be taken into account.

The sensitivity formula used is presented below. Suppose the signal flowgraph of the filter has an input node **a** and an output node **b**. The sensitivity of the filter transfer function T_{ab} to variations in a branch transmittance F_{nm} (where the branch leaves node n of the graph and enters node m) is

$$\frac{\partial T_{ab}}{\partial F_{nm}} = T_{an}T'_{bm} \qquad (4.13)$$

where T_{an} is the system function from node **a** to node n, and T'_{bm} is the system function from node **b** to node m in the transposed signal flowgraph (i.e. a new signal flowgraph obtained simply by reversing the direction of each branch. This result can be obtained using the generalisation of Tellegen's theorem presented in [172].

The transposed network corresponds to a new switched- capacitor filter with the input connected to earth, and with the input capacitor on the final filter section switched between the output of the penultimate stage and the new input, instead of between the penultimate stage output and earth. The equivalent circuit of this filter corresponds to that of the original, but with the input voltage (current)

applied in series with the load termination instead of in series with the source termination, and with the output being the current through (voltage across) the source termination for an odd (even) order filter. The equivalent circuit is illustrated for the odd order case in Fig. 4.2. For the original circuit, the transfer function is $H = i_l/v_S$ with v_l set to zero, and for the circuit corresponding to the transposed signal flowgraph of the filter, the transfer function is $H = i_S/v_l$ with v_S set to zero.

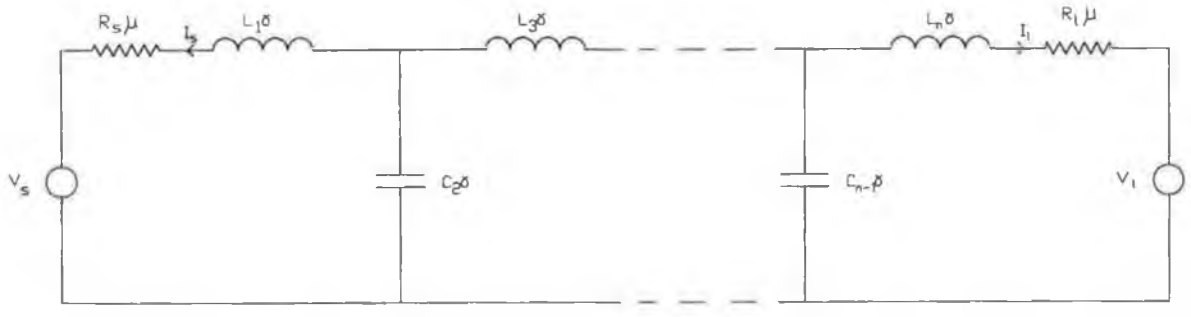


Fig. 4.2: Equivalent circuits for original and transposed filters - odd order case.

Thus, in order to evaluate the sensitivity of the filter transfer function to variations in any element value, only two circuit analyses are required at a given frequency. The analysis must nevertheless be performed efficiently if computation time is not to be excessive, in which case another technique for evaluating filter sensitivity would be preferred.

4.3: Evaluation of the Amplitude Sensitivity.

4.3.1: Frequency Domain Analysis of the SC Filter.

The technique used in analysing the circuit is as follows:

The output voltages of the filter sections are chosen as state variables, and a state-space description of the filter is obtained of the form

$$\underline{A}\ \underline{v} = \underline{B}\ v_{in} \tag{4.14}$$

where

$$\underline{A} = \begin{vmatrix} z_1 & 1 & 0 & 0 & \ldots\ldots & 0 \\ -1 & z_2 & 1 & 0 & \ldots\ldots & 0 \\ 0 & -1 & z_3 & 1 & & . \\ . & & . & . & . & . \\ . & & & . & . & . \\ . & & & & . & . \\ . & & & & -1 & z_{n-1} \quad 1 \\ 0 & 0 & \ldots\ldots & .0 & -1 & z_n \end{vmatrix} \tag{4.15}$$

$$\underline{v} = [v_1\ v_2\ \ldots\ldots\ v_n]' \tag{4.16}$$

$$\underline{B} = [1\ 0\ 0\ \ldots\ldots\ldots\ 0]' \tag{4.17}$$

where z_i corresponds to the impedance or admittance in the corresponding branch of the equivalent circuit, i.e.

$$\begin{aligned} z_1 &= L_1\gamma + R_S\mu \\ z_i &= L_i\gamma \quad ,1 < i < n,\ i \text{ odd} \\ z_i &= C_i\gamma \quad ,1 < i < n,\ i \text{ even} \\ z_n &= L_n\gamma + R_1\mu, \qquad n \text{ odd} \\ z_n &= C_n\gamma + G_1\mu, \qquad n \text{ even}. \end{aligned} \tag{4.18}$$

At any given normalised frequency $\theta = \pi f/f_S$, the state variable vector $\underline{v}$ can be evaluated for a unit input at that frequency as described below.

Evaluate the z_i's at frequency θ, using $\mu \rightarrow \cos\theta$, $\gamma \rightarrow j\sin\theta$.
Arbitrarily assume that the output $v_n = 1$.
Hence v_{n-1} can be calculated using

$$-v_{n-1} + z_n\ v_n = 0 \tag{4.19}$$

Similarly, for i = n-2 down to i = 1, v_i can be found as

$$v_i = z_{i+1}\ v_{i+1} + v_{i+2} \tag{4.20}$$

The input required to produce a unit output is thus

$$v_{in} = z_1 v_1 + v_2 \tag{4.21}$$

It follows that the state variable vector for a unit input has the value $\underline{y}/v_{in}$, where the values of $\underline{y}$ and v_{in} are calculated as above.

The response for the transposed signal flowgraph can be found using (4.14) by modifying $\underline{A}$ and $\underline{B}$ in (4.15) and (4.17) as follows:

$$\underline{A} \rightarrow \underline{A}'$$
$$\underline{B} \rightarrow [0\ 0\ .....\ 0\ 1]'$$

4.3.2: Calculating Sensitivity from the Frequency Domain Analysis.

The transmissions of the branches which have v_i as output are of the form z_i^{-1}. Suppose one such branch leaves node n and enters node m. Then, using (4.13),

$$\frac{\partial T_{ab}}{\partial (z_i^{-1})} = T_{an} T'_{bm} \tag{4.22}$$

where a,b are the input and output nodes respectively, T_{an} is the systen function from the input to node n, and T'_{bm} is the system function (for the transposed signal flowgraph) from the output (which becomes the new input in the transposed graph) to node m.

Evidently, the system responses with output v_i (i.e. those actually calculated using (4.14)) in the original and transposed flowgraphs are T_{am} and T'_{bn} respectively, since the branch of transmission z_i^{-1} enters node n in the original network, and node m in the transposed network.

However

$$\frac{\partial T_{ab}}{\partial (z_i)} = \frac{\partial T_{ab}}{\partial (z_i^{-1})} \frac{\partial (z_i^{-1})}{\partial (z_i)}$$

$$= - \frac{1}{z_i^2} \frac{\partial T_{ab}}{\partial (z_i^{-1})}$$

$$= - z_i^{-2} T_{an} T'_{bm} \tag{4.23}$$

but, evidently, by inspecting the signal flowgraph for filters of the type being discussed, since the only branch entering node m (node n) in the original (transposed) signal flowgraph is that with transmission z_i^{-1}, then

$$T_{am} = z_i^{-1} T_{an}$$
$$T'_{bn} = z_i^{-1} T'_{bm} \tag{4.24}$$

so

$$\frac{\partial T_{ab}}{\partial (z_i)} = T_{am} T'_{bn} = - v_i v'_i \tag{4.25}$$

where v_i and v'_i are calculated as described earlier for the original and transposed signal flowgraphs respectively.

4.3.3: Amplitude Sensitivity to Element Values.

The technique described above is completely general, and can be applied to any network whose signal flowgraph can be described by (4.14)-(4.17). For the present application, the required sensitivities are $\partial / \partial x (|T|^2)$ and $\partial / \partial r (|T|^2)$ where $T = T_{ab}$ and the z_is are of the form

$$z_i = r \cos\theta + j \, x \sin\theta \tag{4.26}$$

which is equivalent to (4.18) evaluated at physical frequencies.

Thus a formula is required relating $\partial/\partial u(|T|^2)$ and $\partial/\partial z(T)$, where z is a function of u, with u real.

The system response T can be written in terms of its (real) amplitude and phase responses as $T = A\, e^{j\Phi}$ where A and Φ are real functions of u, so

$$\partial/\partial u(T) = e^{j\Phi} \left[\partial/\partial u(A) + j\, A\, \partial/\partial u(\Phi) \right] \tag{4.27}$$

or

$$e^{-j\Phi}\, \partial/\partial u(T) = \left[\partial/\partial u(A) + j\, A\, \partial/\partial u(\Phi) \right] \tag{4.28}$$

Now, since A,Φ and u are all real, it follows that

$$\begin{aligned} \partial/\partial u(A) &= \mathrm{Re}\left[e^{-j\Phi}\, \partial/\partial u(T) \right] \\ &= A^{-1}\, \mathrm{Re}\left[T^*\, \partial/\partial u(T) \right] \end{aligned} \tag{4.29}$$

Also, given that $\partial/\partial u(|T|^2) = 2\,|T|\,\partial/\partial u(|T|)$, and that $|T| = A$, then

$$\partial/\partial u(|T|^2) = 2\,\mathrm{Re}\left[T^*\, \partial/\partial u(T) \right] \tag{4.30}$$

Further noting that $\partial/\partial u(T) = \partial/\partial z(T)\, \partial/\partial u(z)$, then

$$\partial/\partial u(|T|^2) = 2\,\mathrm{Re}\left[T^*\, \partial/\partial z(T)\, \partial/\partial u(z)\right] \tag{4.31}$$

If $u = r$ then $\partial/\partial u(z) = \cos\theta$ so

$$\partial/\partial r(|T|^2) = 2\cos\theta\,\mathrm{Re}\left[T^*\, \partial/\partial z(T)\right] \tag{4.32}$$

If $u = x$ then $\partial/\partial u(z) = j\sin\theta$ so

$$\partial/\partial x(|T|^2) = -2\sin\theta\,\mathrm{Im}\left[T^*\, \partial/\partial z(T)\right] \tag{4.33}$$

Thus the sensitivities of the squared-amplitude response to the terminations are

$$S^{|T|^2}_{R_s} = - \frac{2 R_s}{|T|^2} \cos\theta \, \mathrm{Re}[\, T^* \, v_1 \, v_1' \,] \tag{4.34}$$

$$S^{|T|^2}_{R_l} = - \frac{2 R_s}{|T|^2} \cos\theta \, \mathrm{Re}[\, T^* \, v_n \, v_n' \,] \tag{4.35}$$

R_l is replaced by G_l in (4.35) for even-order filters. The sensitivities to variations in the inductor and capacitor values are

$$S^{|T|^2}_{L_i} = \frac{2 L_i}{|T|^2} \sin\theta \, \mathrm{Im}[\, T^* \, v_i \, v_i' \,] \tag{4.36}$$

$$S^{|T|^2}_{C_i} = \frac{2 C_i}{|T|^2} \sin\theta \, \mathrm{Im}[\, T^* \, v_i \, v_i' \,] \tag{4.37}$$

Evidently, the sensitivities to the actual capacitor ratios in the implemetation are easily obtained, since $R \rightarrow C_3/C_1$ and $L \rightarrow (2C_2 + C_3)/C_1$, so, setting $C_1 = 1$ results in

$$\frac{\partial |T|^2}{\partial C_3} = \frac{\partial |T|^2}{\partial R} + \frac{\partial |T|^2}{\partial L} \tag{4.38}$$

$$\frac{\partial |T|^2}{\partial C_2} = 2 \frac{\partial |T|^2}{\partial L} \tag{4.39}$$

Equivalent formulae obviously hold for capacitance ratios derived from capacitor and conductance values.

4.4: Sensitivity Properties of SC Ladder Filters.

The synthesis program of Chapter Three has been extended to include the above technique for sensitivity evaluation.

Considering the case of an equiripple passband approximation, it is

expected that the passband sensitivity of the switched- capacitor filters are inferior to those of the equivalent passive filters. The reasoning behind this expectation is given below.

The squared-amplitude response of the filter is denoted by $|H_{21}|^2$. For conventional passive ladder filters, the transducer power gain is related to $|H_{21}|^2$ by

$$|S_{21}|^2 = 4\ (r_S/r_1)\ |H_{21}|^2 \tag{4.40}$$

Thus the maxima of $|S_{21}|^2$ and $|H_{21}|^2$ co-incide. However, for switched-capacitor filters of the type in [76], because of the frequency variation of the terminations, (4.40) becomes

$$|S_{21}|^2 = 4\ (r_S k_1)\ |\mu H_{21}|^2 \tag{4.41}$$

where $k_1 = \eta_1$ for an odd order filter, and $k_1 = g_1$ for even orders. This is the same expression as obtained for the transducer power gain of the auxiliary network in [76]. It follows that, if the filter is designed for an equiripple passband, then maximum power transfer will occur only at d.c. for an odd order filter, and at no frequency for an even order filter, because the factor $|\mu|^2 = \cos^2\theta$ decreases monotonically from $\theta = 0$ to $\theta = \pi/2$. Since the argument for low passband sensitivity is based on the assumption that the transducer power gain is unity at some frequencies in the passband, it is not valid for filters of the type in [76].

The filters in [92], on the other hand, which use the special input stage of Fig. 2.4, have a transfer function of the form μH_{21}, where H_{21} is the transfer function of the corresponding filters discussed in [76] (i.e. where $C_1 = 0$ in Fig. 2.4, so that the input stage is a conventional d.d.i.), and so can be designed to have a unity transducer power gain where the peaks in the amplitude response occur. However, the factor μ is realised by the special feed-in branch at the filter input, the amplitude sensitivity of which is estimated below. The filter effectively consists of the cascade of two filters, with amplitude responses $|T_1|^2$ and $|T_2|^2$, where T_2 is the transfer function of the ladder, and T_1 is the transfer function of the feed-in branch which, to within a constant delay, is of the form

$$T_1(z) = 1 + C_1 z^{-1} \tag{4.42}$$

with C_1(nominal) = 1. This means that the two capacitors used to implement the feed-in branch are nominally equal in value. Clearly

$$\frac{\partial |T|^2}{\partial C_1} = |T_1|^2 \frac{\partial |T_2|^2}{\partial C_1} + |T_2|^2 \frac{\partial |T_1|^2}{\partial C_1} \tag{4.43}$$

Assuming that the filter is designed with $R_S = R_l = 1$, assuming that the first term on the right-hand side of (4.43) is zero, observing that $|T_2|^2 = (\cos^2\theta)/4$ at a point of maximum power gain, and evaluating the second term for $C_1 = 1$ yields the result

$$\frac{\partial |T|^2}{\partial C_1} = 1 \tag{4.44}$$

at a point of maximum power transfer. Thus the filters of [92] achieve a low sensitivity to the other capacitance ratios in the passband, at the expense of a high sensitivity to the capacitance ratio in the feed-in branch.

4.5: A Filter Response Featuring Equiripple Transducer Power Gain in the Passband.

To numerically verify that the filters of [76] do not achieve the minimum possible sensitivity when designed to achieve a transfer function with an equiripple passband, it is necessary to calculate their sensitivities for such a transfer function, and for a transfer function which results in an equiripple transducer power gain in the equivalent circuit (or equivalently in the auxiliary network) of the filter, since such a response is expected, *a priori*, to feature the lowest sensitivity.

The auxiliary network described in Chapter Three is equivalent, for an n-th order filter, to n-1 unit elements followed by a series short-circuited stub. The amplitude response which results in an equiripple passband for such a network is known to be given by [74,82]

$$|S_{21}(\theta)|^{-2} = 1 + \epsilon^2 F_n^2(\theta) \tag{4.45}$$

where

$$F_n(\theta) = \cosh((n-1)\Phi + \eta)$$
$$= \cosh(n-1)\Phi\cosh\eta + \sinh(n-1)\Phi\sinh\eta \qquad (4.46)$$

with

$$\cosh \Phi = \sin\theta/\sin\theta_0 \qquad (4.47)$$
$$\cosh \eta = \tan\theta/\tan\theta_0 = \Omega/\Omega_0$$

To synthesise a filter with this magnitude response, a rational expression in λ for $S_{11}(\lambda)S_{11}(-\lambda)$ is required. It is first noted that

$$\cosh (n-1)\Phi = T_{n-1}(\sin\theta/\sin\theta_0) \qquad (4.48)$$

and

$$\sinh (n-1)\Phi = \left[\left|\frac{\sin\theta}{\sin\theta_0}\right|^2 - 1\right]^{\frac{1}{2}} \quad f_{n-2}\left[\frac{\sin\theta}{\sin\theta_0}\right| \qquad (4.49)$$

where $T_n(x)$ is the Chebyshev polynomial of the first kind of order n in x, and $f_{n-2}(x)$ is a polynomial in x which is constructed using the same recursive formula as $T_n(x)$, but with the initial conditions $f_0(x) = 1$, $f_1(x) = 2x$.

The following identities are also noted

$$\sinh \eta = ((\Omega/\Omega_0)^2 - 1)^{1/2} \qquad (4.50)$$

and

$$(\sin\theta/\sin\theta_0)^2 - 1 = (1+\Omega^2)^{-1}((\Omega/\Omega_0)^2 - 1)^{1/2} \qquad (4.51)$$

where $\Omega = \tan\theta$. Using (4.48)-(4.51), the expression for $F_n(\theta)$ may be written

$$F_n(\theta) = (\Omega/\Omega_0)T_{n-1}(\sin\theta/\sin\theta_0)$$
$$+ (\Omega^2-\Omega_0^2)/\Omega_0 \ (1+\Omega^2)^{-1/2} \ f_{n-2}(\sin\theta/\sin\theta_0) \qquad (4.52)$$

or, writing $\Omega = \sin\theta \ (1+\Omega^2)^{1/2}$

$$F_n(\theta) = (1+\Omega^2)^{1/2}/\Omega \; [\; \sin\theta \; T_{n-1}(\sin\theta/\sin\theta_o) + (\Omega^2-\Omega_o^2) \; (1+\Omega^2)^{-1} \; f_{n-2}(\sin\theta/\sin\theta_o) \;] \qquad (4.53)$$

For n even, $T_{n-1}(\sin\theta/\sin\theta_o)$ may be written in the form

$$T_{n-1}(\sin\theta/\sin\theta_o) = \sin\theta \; (1+\Omega^2)^{(n-2)/2} \; T_e(\Omega^2) \qquad (4.54)$$

where $T_e(\Omega^2)$ is a polynomial in Ω^2 of order (n-2)/2. Similarly, $f_{n-2}(\sin\theta/\sin\theta_o)$ may be written as

$$f_{n-2}(\sin\theta/\sin\theta_o) = (1+\Omega^2)^{(n-2)/2} \; f_e(\Omega^2) \qquad (4.55)$$

where $f_e(\Omega^2)$ is also a polynomial in Ω^2 of order (n-2)/2. Hence $F_n(\theta)$ may be written, for even n, as

$$F_n(\theta) = \frac{\Omega^2 T_e(\Omega^2) + (\Omega^2 - \Omega_o^2) \; f_e(\Omega^2)}{\Omega_o \; (1 + \Omega^2)^{(n-1)/2}} \qquad (4.56)$$

For n odd, $T_{n-1}(\sin\theta/\sin\theta_o)$ may be written in the form

$$T_{n-1}(\sin\theta/\sin\theta_o) = (1+\Omega^2)^{(n-1)/2} \; T_o(\Omega^2) \qquad (4.57)$$

where $T_o(\Omega^2)$ is a polynomial in Ω^2 of order (n-1)/2. Similarly, $f_{n-2}(\sin\theta/\sin\theta_o)$ may be written as

$$f_{n-2}(\sin\theta/\sin\theta_o) = \sin\theta \; (1+\Omega^2)^{(n-3)/2} \; f_o(\Omega^2) \qquad (4.58)$$

where $f_o(\Omega^2)$ is also a polynomial in Ω^2, of order (n-3)/2. Hence $F_n(\theta)$ may be written, for odd n, as

$$F_n(\theta) = \frac{\Omega T_o(\Omega^2) + \Omega(\Omega^2 - \Omega_o^2) \; f_o(\Omega^2)}{\Omega_o \; (1 + \Omega^2)^{(n-1)/2}} \qquad (4.59)$$

Having obtained $F_n(\theta)$ as a quasi-rational function of Ω, it follows that

$$S_{11}(\lambda)S_{11}(-\lambda) = \frac{\epsilon^2\, g(\lambda)}{(1 - \lambda^2)^{n-1} + \epsilon^2\, g(\lambda)} \tag{4.60}$$

where $g(\lambda)$ is given by

$$g(\lambda) = \Omega_0^{-2}[-\lambda^2 T_e(-\lambda^2) - (\lambda^2+\Omega_0^2) f_e(-\lambda^2)],\ n \text{ even}$$
$$g(\lambda) = -\lambda^2\Omega_0^{-2}[T_0(-\lambda^2) - (\lambda^2+\Omega_0^2) f_0(-\lambda^2)],\ n \text{ odd} \tag{4.61}$$

Having obtained $S_{11}(\lambda)S_{11}(-\lambda)$ in this form, as a rational function of λ^2, the filter may then be synthesised using the techniques of Chapter Three. This approximation type has been implemented in the synthesis software described in the last chapter. Because it features an equiripple transducer power gain, its passband sensitivity is expected to be lower than that of the standard equiripple response.

4.6: Results Obtained.

The sensitivities of filters of the type in [76] have been evaluated for an equiripple passband response, and an equiripple passband transducer gain. The sensitivity plots obtained are now compared for a ninth-order filter, with the same filter specifications as chosen in Chapter Three for evaluating the synthesis technique.

The response of the filter designed for an equiripple amplitude response in the passband is thus that shown in Fig. 3.17. The required passband response for the filter with an equiripple transducer power gain in the passband, as determined using (3.35), is shown in Fig. 4.3. The peaks in this response correspond to points of maximum power transfer, and occur at, approximately, f/f_s = 0.00, 0.20, 0.39, 0.54, and 0.60 respectively. The actual passband response of the synthesised filter is shown in Fig. 4.4. Clearly the two responses are in excellent agreement. This filter exhibits an amplitude response which closely resembles that of an equiripple-passband filter, but where the gain increases with frequency in the passband, compared with that obtained, for example in Fig. 3.17, because the squared- amplitude response equals the equiripple transducer power gain multiplied by a factor $\cos^{-2}\theta$.

The sensitivity of the squared-amplitude response in the passband to variations in the value of L_1, the first inductor in the equivalent circuit of Fig. 3.7(a), is shown in Fig. 4.5 for an equiripple passband transfer function, and in Fig. 4.6 for an equiripple passband transducer power gain. The sensitivity in Fig. 4.5 is zero at the origin, and at frequencies of approximately $0.12f_S$ and $0.2f_S$. Thereafter in the passband, the sensitivity is non-zero and positive. In contrast, the sensitivity in Fig. 4.6 is zero at seven points in the passband, five of these corresponding to points of maximum transducer power gain, and two at approximately $f = 0.12f_S$ and $f = 0.35f_S$. Also the variation in the sensitivity appears less pronounced.

The corresponding sensitivities for the first capacitor, C_2, are shown in Figs. 4.7 and 4.8. Here the improved sensitivity performance for the filter with equiripple passband transducer power gain , shown in Fig. 4.8, is less dramatic, since the sensitivity passes through zero five times for the filter with equiripple passband amplitude response, as shown in Fig. 4.7. However, the variation in sensitivity with frequency is again lower for Fig. 4.8 than for Fig. 4.7. Note that the expected sensitivity zero at a frequency of approximately $0.6f_S$ appears to be absent from Fig. 4.8. This is simply a consequence of the limited plotting resolution available in plotting Fig. 4.8.

Similar results are obtained for the other elements in the equivalent circuit, with the exception of the terminations, which, for example, have a sensitivity of unity at d.c. It can be seen that, as expected, the switched- capacitor ladder features low sensitivity, but that, as a consequence of the frequency variation in the value of the terminations in the equivalent circuit, this sensitivity is not as low as might be expected from an analysis which makes the approximation that the terminations are frequency-independent. As demonstrated by the results presented here, this effect is not of major consequence for low pass filters, where, in the passband, $\cos\theta \simeq 1.0$, but it may seriously degrade the sensitivity properties of other filter types, notably high-pass filters.

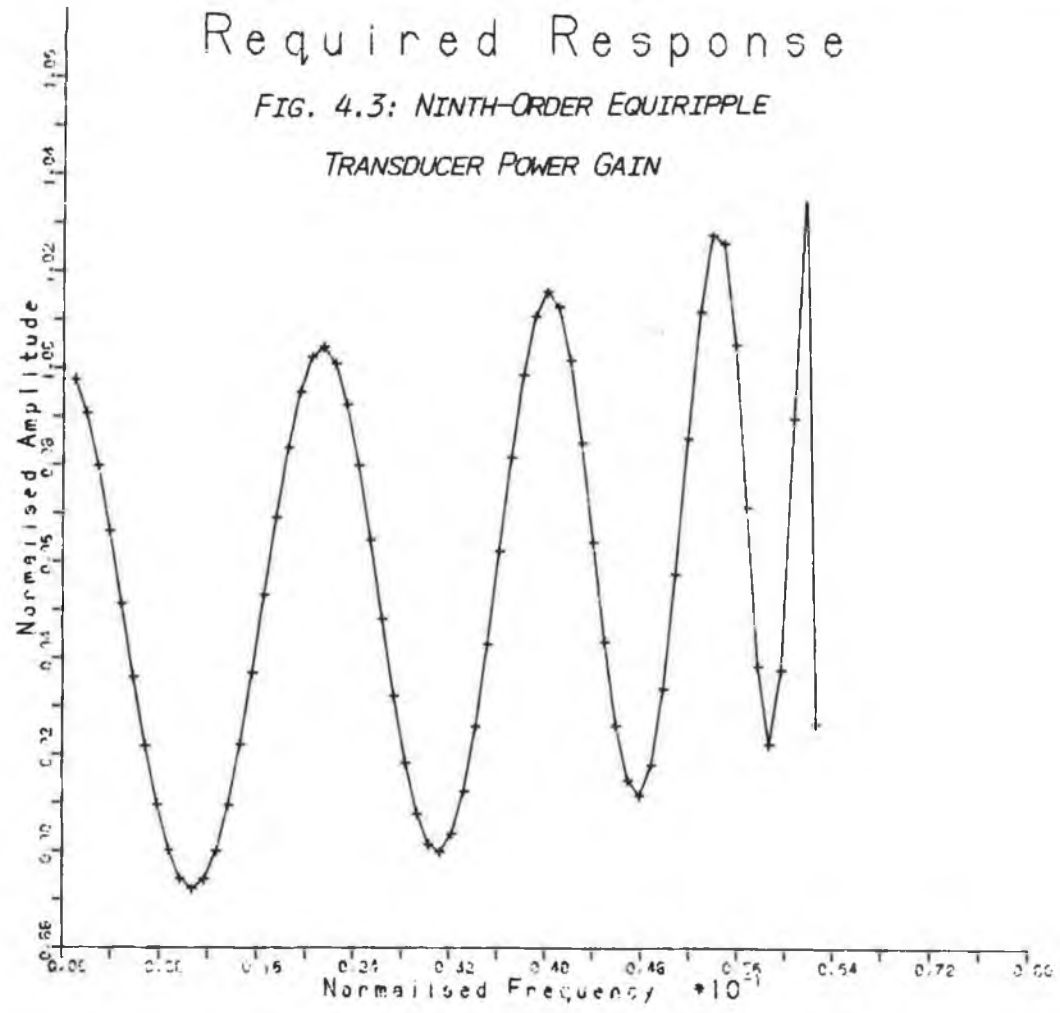


FIG. 4.3: NINTH-ORDER EQUIRIPPLE TRANSDUCER POWER GAIN

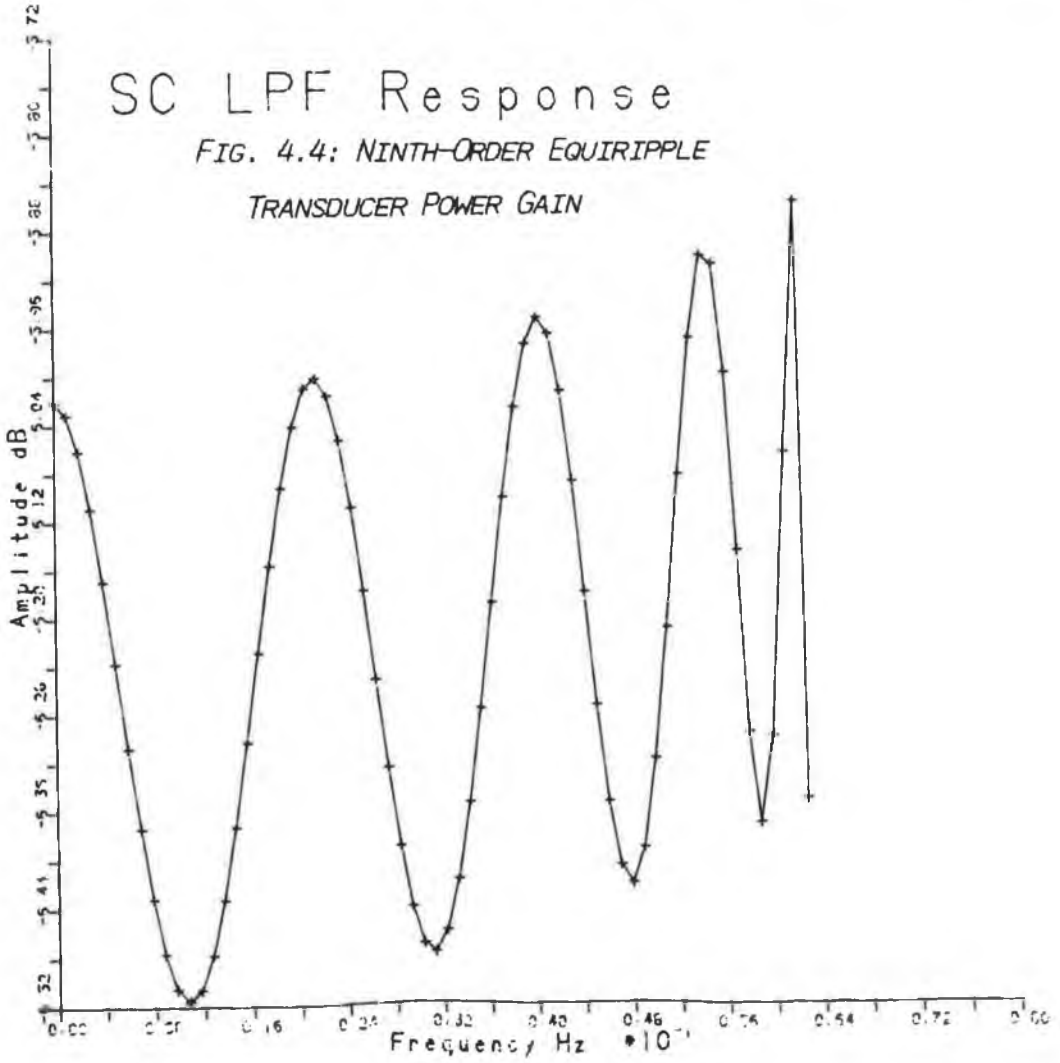


FIG. 4.4: NINTH-ORDER EQUIRIPPLE TRANSDUCER POWER GAIN

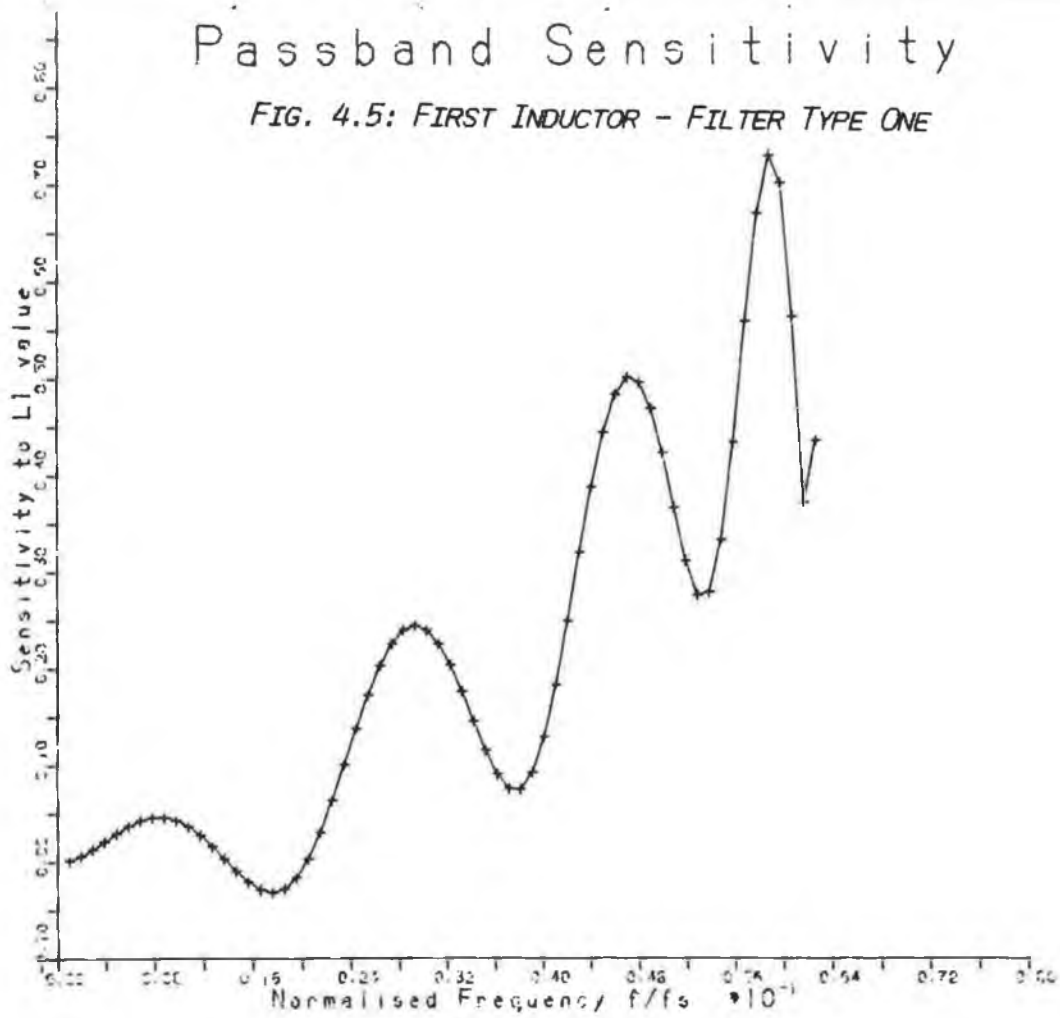


FIG. 4.5: FIRST INDUCTOR - FILTER TYPE ONE

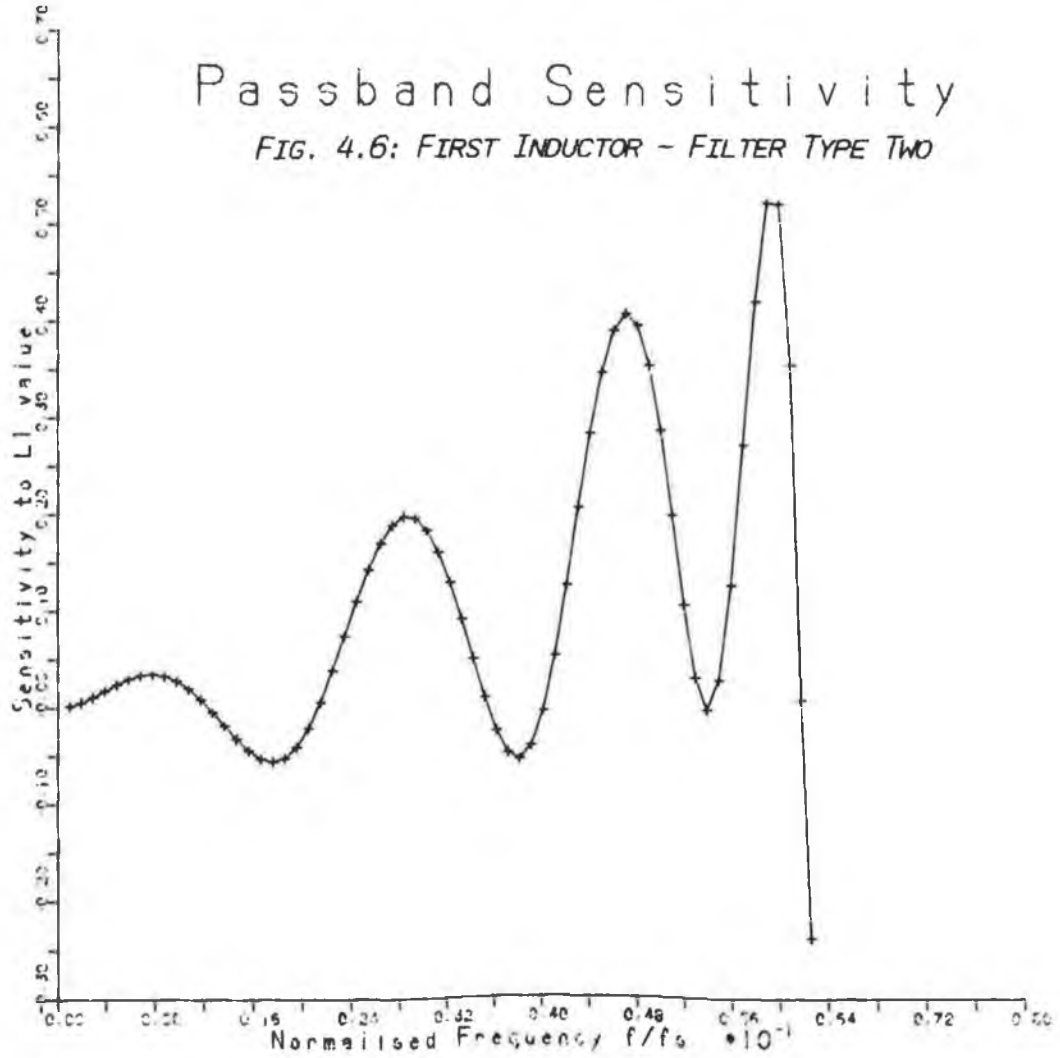


FIG. 4.6: FIRST INDUCTOR - FILTER TYPE TWO

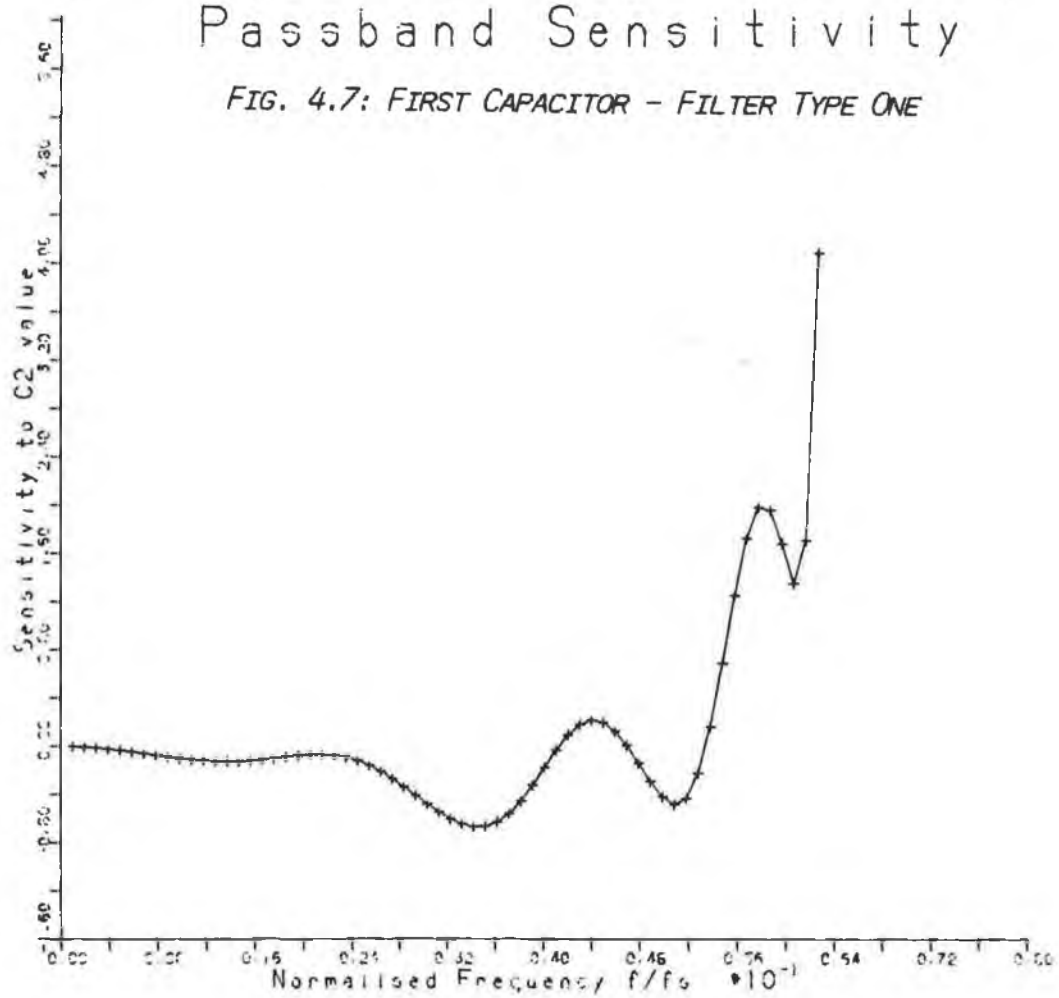


FIG. 4.7: FIRST CAPACITOR - FILTER TYPE ONE

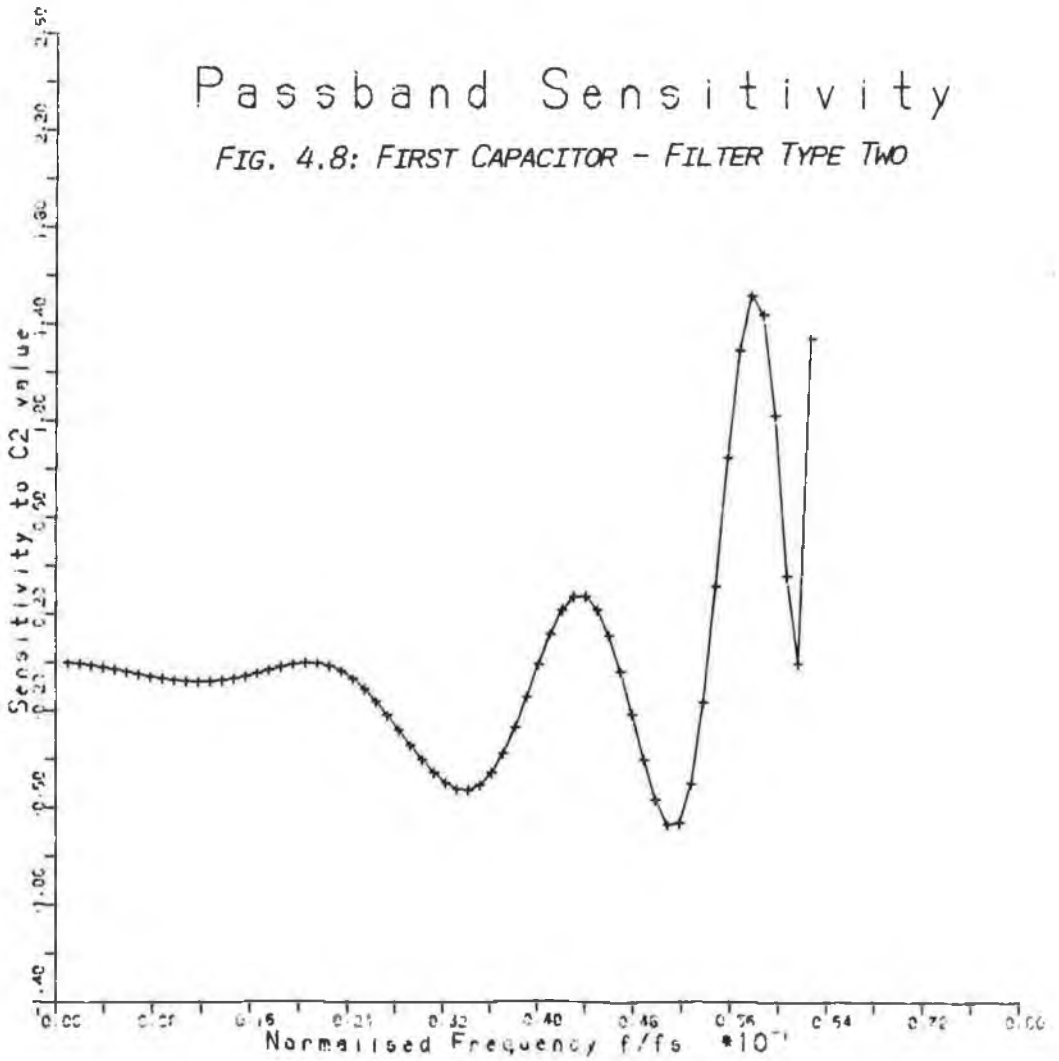


FIG. 4.8: FIRST CAPACITOR - FILTER TYPE TWO

Chapter Five: SCF STRUCTURES FOR EXTENDED FREQUENCY RANGE OPERATION

5.1: Introduction.

The frequency range over which a practical switched- capacitor filter can operate is limited. These limitations arise because the op-amps, switches, capacitors and interconnections used are not ideal. The magnitude of the non-idealities are dependent on the process used to fabricate the switched- capacitor filter. Thus, for instance, it would be expected that the *gain-bandwidth product* of an op-amp implemented using a 1.5 μm process (i.e. a process where the minimum feature size is 1.5 μm) would be higher than that of an op-amp implemented with a 5 μm process. The effect of many of these non-ideal factors is reduced as the feature size of the process is reduced. The values of parasitic resistances and capacitances would be reduced, for example, so that, for a given unit capacitor size, their influence on charge transfer through the filter is reduced as their values are scaled downwards. However, the current state of the art in MOS technology is a feature size of 1-2 μm, and considerations of cost or availability may dictate the use of a process with a more conservative feature size. Thus it is often necessary, when designing a switched- capacitor filter for high frequency operation, to choose a filter topology which is more robust with respect to process limitations than the traditional structures used for voice-band applications. In this context no absolute frequency range is implied by the term 'high frequency operation'. Rather the term is used to denote the frequency range beyond which the approximations usually used in the design procedure (e.g. that the op-amp gain is independent of frequency) can no longer be regarded as valid for a switched- capacitor filter fabricated on the MOS process being considered.

5.2: Technological Considerations for High Frequency SCFs.

Formulae for the effect of finite gain-bandwidth on the performance of the conventional types of LDI-based integrators are given in [60]. One of the principal factors limiting the performance of a switched- capacitor filter at high frequencies is the op-amp *settling time* [59,69]. The settling time of an op-amp, in the context of a switched - capacitor system, is the time taken for the op-amp output to settle (i.e. for the output voltage to attain, to within a specified tolerance dictated by permissible distortion levels, the value towards which it is asymptotically converging during the current clock phase, assuming constant system

inputs). The settling time is dependent on the *slew-rate* and gain-bandwidth of the op-amps, and on the topology of the circuit in which they are connected. Improved op-amp design, optimised for high-speed operation, can increase slew-rate and gain-bandwidth up to a point. Further improvements where possible can be made by circuit modifications which reduce the extent to which signals propagate through the filter on each phase.

For example, consider the circuit shown in Fig. 5.1. This is the general SC biquad introduced by Fleischer and Laker [23], which is based on the lossless discrete integrator as a substructure and which has seen extensive use wherever a switched-capacitor biquad is required [e.g. 149,155,173]. Similar biquad structures have been proposed by other authors [e.g. 9,19,20]. However circuits of this type are not optimal with regard to settling time requirements for three reasons :

1) Unswitched capacitors such as 'E ' in Fig. 5.1 are used. The use of such capacitors, which in theory add a simple gain term to the expression for the integrator output, will, in general, result in lengthened settling times because they provide a permanent path for the transfer of charge from one node of the network to another. Thus , in Fig. 5.1 OA_1 and OA_2 are always interconnected via capacitor 'E', so that the dynamics governing the settling time are more complex than would otherwise be the case.

2) Where the output of one op-amp is applied as an input for another, the outputs of both op-amps are updated on the same phase. In Fig. 5.1 settling time would be reduced if the output of OA_2 was held during the phase when OA_1 reads the OA_2 output via switched capacitor 'C ', since the two op-amp outputs would then settle alternately rather than simultaneously.

3) The standard inverting integrator of [9], which features a delay-free path from input to output, is used. Capacitors 'G' , 'I' and 'C' in Fig. 5.1 provide signal inversion, essential so as to provide negative feedback, in this way, but require, for example, the OA_1 output to settle to the required value while 'G', 'I', and 'C' are being charged, rather than after the charge on these capacitors has stabilised.

The presence of the above three conditions indicates a network which

on either or both phases (assuming a standard two-phase clock) retains a complex topology, which, it is apparent from a consideration of charge flow, will result in a lengthy response time to transients in the practical situation where circuit elements are non-ideal. Conversely, if, during each phase, the network would be so disconnected that no path for charge flow would exist from one op-amp to any other, then the settling times for each op-amp output would be independent.

It can parenthetically be noted that the circuit of Fig. 5.1 will often require three op-amps, since it requires the input to be sampled and held over one full clock period, which may require additional circuitry.

5.3: Techniques for Extending SCF Frequency Range.

Several approaches are possible in reducing settling time requirements.

5.3.1: Compensation.

The equivalent problem for RC-active filters can be solved by analysing the effects of non-ideal circuit operation, and adjusting the element values to account for these non-idealities, i.e. the filter design is 'pre-warped' to account for finite gain-bandwidth effects. The performance of such filters deteriorates progressively with increasing frequency. However, SC filters do not feature such 'graceful degradation '. The step responses for the op-amp outputs in a switched- capacitor filter can, to a first order, be approximated as exponential curves, equivalent to the voltage across a capacitor being charged by a resistive voltage source. The fraction of the required charge which is actually transferred to such a capacitor obviously falls rapidly as the charge time is reduced through the value of the time constant for the circuit. In fact, as the clock rate is increased , switched- capacitor filter performance degrades rapidly over a short frequency range, and high-Q bandpass filters can , for example, become unstable [62]. Because of this sensitivity, this approach is not feasible when applied to SC filters.

An alternative approach is to physically compensate for the errors in charge transfer within an integrator at high frequencies by the introduction of additional compensation circuitry [174]. Since this approach requires several additional op-amps per integrator, it represents a considerable increase in circuit complexity.

5.3.2: Double-Sampling.

One approach which has been successful for some circuit topologies is the use of a double-sampling scheme [78]. Fig. 5.2 shows a damped discrete integrator modified so as to incorporate double sampling. The double sampling approach involves replicating the switched-capacitor circuitry but connecting it to the opposite phase. Then the *even* and *odd* circuits (i.e. the circuits as connected during φ_2 and φ_1 respectively) are identical. Obviously, for example, this technique cannot be applied to the circuit in Fig. 5.1, where signals are sampled on both clock phases. This replication means that the sampling rate of the system is twice the clock frequency. Hence, for operation in a given frequency range, the clock frequency using double-sampling is one half of that for a conventionally designed filter. Thus the upper limit on operating frequency has been extended without significantly increasing the stringency of the op-amp settling time requirement. This benefit has been obtained , however , at the price of doubling the number of switched capacitors and switches in the circuit, thus considerably increasing the chip area occupied by the filter.

5.3.3: Fully Differential Operation.

Other approaches to improving the frequency response of the switched-capacitor filter involve the use of a fully differential filter structure [59,126,140,141]. A fully differential architecture also brings other benefits [137] such as increasing the dynamic range by increasing the voltage capability and (when used with chopper-stabilised op-amps) reducing 1/f noise. A fully differential structure will also reduce the effects of *clock feedthrough* and increase power supply rejection, since, to a first order, these noise signals represent a common-mode input to the differential filter and will be suppressed. Thus there are considerable benefits to be obtained from the choice of a fully differential structure. It has been shown [59] that this structure also leads to improved high frequency performance. The penalty paid for this is an increase of close to one hundred per cent in die area required, since all capacitors and switches must be duplicated, and a fully differential op-amp requires almost as much area as two conventional op-amps. However the presence of complementary outputs in the fully differential op-amp allows circuit topologies which would otherwise require additional inverting stages to be used. This circuit flexibility can make the fully differential structure more economical than the double-sampling scheme in some applications. In

particular, such a structure allows circuits which avoid the three conditions which degrade settling time to be designed. For this reason the differential structure will be examined in further detail.

Fig. 5.3a shows the structure of a conventional (or *single-ended*) non-inverting lossless discrete integrator. Fig. 5.3b shows the corresponding circuit for a fully differential (or *double-ended*) integrator. The values for C_1 and C_2 are identical in both circuits. A more complex single-ended circuit, such as a biquad, can readily be converted to a fully differential structure by replacing the single-ended integrator sections with double-ended equivalents, using the approach shown in Fig. 5.3. This results in a double-ended filter with the same transfer function as the prototype, since the transfer functions of the integrator sections remain unchanged. This identity of transfer functions is widely assumed in the literature, but a formal proof does not appear to have been published to date. Such a proof is given in Appendix A which considers non-inverting and inverting integrators for both the damped and lossless cases. In addition, the transfer function of the differencing-input integrator [59,126] of Fig. 5.4 is derived. It is shown that the differencing-input integrator requires input capacitors of half the value for the corresponding single-ended type.

The advantages of fully differential circuitry for high frequency operation of switched-capacitor filters will now be summarised [59,140] :

1) Because the signal paths are fully differential, the differential-to-single-ended conversion required within single-ended op-amps is avoided. This simplification means that the op-amp bandwidth will exceed that of the corresponding single-ended design.

2) For high frequency operation, the charging time constants for the capacitors must be minimised, to ensure that charge is properly transferred through the circuit. Therefore the on-resistance of the switching transistors must be reduced, compared with the values for voice-band filters. This is achieved by increasing the transistor size. Unfortunately this increases the amount of clock feedthrough present in the signal path. Thus a filter structure which suppresses clock feedthrough is required. Also, the sizes of capacitors are reduced. This increases the effect of stray capacitances and thus reduces power supply rejection. The differential structure features improved power supply rejection, as already stated.

3) The filter sampling rate must be as low as possible, since this will reduce op-amp settling time and will also in general result in a design with reduced capacitance ratio spread , thereby reducing charging time constants. A low sampling rate however means that the filter passband occupies a greater proportion of the frequency range from zero to the Nyquist rate than would otherwise occur. It follows that the amount of noise aliased into the passband will be increased for such filters. This is another reason for preferring a filter structure which suppresses noise.

5.3.4: Use of Differencing-Input Integrators.

In addition to the above advantages it has been shown by Ribner and Copeland [59] using simulations of non-ideal filters, confirmed by measurement of fabricated filters, that fully differential integrators, when coupled together to form biquadratic sections, diverge less rapidly from ideal performance as signal frequency increases than do single-ended designs. The differencing-input integrator of Fig. 5.4 is particularly suitable, since the input capacitors are halved in value compared with the other integrator types. This reduction in input capacitance brings a number of benefits [59] :

1) The charging time constant for the input capacitors is reduced.

2) The amount of feedback from the op-amp output to its input is reduced. A large feedback loop gain causes longer settling times, and also increases the effect of the finite op-amp gain.

3) The capacitative load presented to each op-amp output in a switched-capacitor filter is reduced. Typically, the designs of op-amp favoured for high frequency switched-capacitor applications, such as the folded cascode [175], feature a high output impedance. For such op-amps, both slew rate and bandwidth improve as the capacitative load is reduced, thereby reducing the settling time.

The results obtained by Ribner and Copeland indicate that, although the use of differencing-input integrators results in the presence of (delay-free) inverting integrator inputs, which, as has been stated earlier, can, in general, be expected to lead to lengthened settling times, the net effect of the use of differencing inputs is to reduce settling times, for the reasons stated above.

5.4: A Switched-Capacitor Filter Structure for High Frequency Applications.

5.4.1: Limitations on the Filter Topology.

For high frequency applications, it is desirable to have a filter structure which offers the versatility of the biquad of Fleischer and Laker, but which is optimally suited for use at higher frequencies. Because of the considerations mentioned above, such a design should fulfil the following requirements :

1) The filter structure should be fully differential.

2) Where possible, differencing-input integrators should be used.

3) The switch phasing should be arranged so that interconnected op-amps do not have outputs which update simultaneously.

4) No unswitched capacitors should be used.

Note that, because of considerations 3) and 4) such a structure could not implement a z-domain transfer function with a second-order numerator using only two op-amps, as does that of Fig. 5.1. This is because there is no delay-free path permissible from the input to the output of the filter, and therefore, writing the numerator of the transfer function as :

$$N(z) = n_2 z^{-2} + n_1 z^{-1} + n_0$$

it follows that $n_0 = 0$, as the impulse response will be zero at time $t = 0$. Thus, the numerator can be, at most, first order, with a delay of one sample period before the filter responds to an input.

To ensure that the transfer function has a second order numerator, it is necessary for three op-amps to be used, if the above constraints are to hold. Thus the Fleischer-Laker biquad cannot simply be modified for double-ended operation to obtain a filter of the required form.

Another difficulty with the circuit of Fig. 5.1 is that it cannot readily be adapted to use differencing-input integrators. To see why this is so, consider the operation of the integrator based around OA_2, with the input from OA_1 removed. This circuit is shown in Fig. 5.5. The difference equation describing the operation of the integrator is :

$$V_o(n)=(F + B)^{-1}(B\ V_o(n-1) - I\ V_{in}(n) + J\ V_{in}(n-\tfrac{1}{2})\ ) \tag{5.1}$$

Assuming that V_{in} is held during φ_1 then :

$$V_{in}(n-\tfrac{1}{2}) = V_{in}(n-1) \tag{5.2}$$

Thus, in the z-domain, the transfer function becomes:

$$V_o(z) = -\ \frac{I - J\ z^{-1}}{F + B - B\ z^{-1}}\ V_{in}(z) \tag{5.3}$$

This transfer function has a zero at z = J/I. However, if Fig. 5.5 is modified to a fully differential structure with differencing inputs, the zero will always occur at z = 1. This is because the operation of the circuit in Fig 5.5 depends on reading the input on both phases, but with different gains. With differencing inputs, the gains on both phases are identical.

5.4.2: Operation of Single-Ended Version of Proposed Filter.

For the above reasons, it is not possible to arrive at a satisfactory filter design by simply modifying Fig. 5.1. Instead, a new topology is required. The single-ended version of this topology is shown in Fig 5.6.

In this design, the first two stages form a standard damped discrete integrator loop, such as might be used in simulating a second order low pass ladder filter. The feedback in the loop is negative as required, because the input from V_2 in the first damped discrete integrator is inverting. The transfer functions from the inputs to V_1 and V_2 have second order denominators, but lower order

numerators, since the technique of Fig. 5.5 has necessarily been avoided. To obtain a second order numerator, the input and the two integrator outputs must be summed. This is done in the third damped discrete integrator, which introduces an additional pole in the transfer function. Thus the transfer function has a second order numerator and a third order denominator. Note that V_{in} is sampled on the same phase by the first and third integrators, so that no sample/hold stage is required at the input. Also, as will subsequently be shown, one of the damping capacitors C_{31} or C_{32} could be removed without lowering the filter order or affecting the range of transfer functions which can be realised. In practice, such an omission generally leads to an increased capacitance ratio spread and total capacitance for the filter.

The transfer function for the filter of Fig 5.6 is derived in Appendix B and is found to be :

$$\frac{V_o(z)}{V_{in}(z)} = \frac{z^{-0.5}\,(a_0 + a_1 z^{-1} + a_2 z^{-2})}{(1 - b_0 z^{-1})\,(b_1 + b_2 z^{-1} + b_3 z^{-2})} \qquad (5.4)$$

where :

$$\begin{aligned}
a_0 &= ka_3 \ ; \\
a_1 &= -\,ka_3(kd_1 + kd_2) + ka_3 ka_2 kb_1 \\
&\quad + kb_3 ka_1 + kc_3 ka_1 ka_2 \ ; \\
a_2 &= ka_3 kd_1 kd_2 - kb_3 ka_1 kd_2 \ ; \\
b_0 &= kd_3 \ ; \\
b_1 &= 1.0 \ ; \\
b_2 &= kb_1 ka_2 - kd_1 - kd_2 \ ; \\
b_3 &= kd_1 kd_2 \ ;
\end{aligned} \qquad (5.5)$$

The k co-efficients are defined in Appendix B. They are all ratios of capacitances, and are thus all positive.

5.4.3: Description of Double-Ended Version of Filter.

Modifying the filter for fully differential operation yields the circuit of Fig. 5.7. Note that, with the exception of that associated with C_{1b3}, all integrator inputs have been replaced by differencing inputs as in Fig. 5.4. An inspection of

Fig. 5.7 indicates that each integrator input (with the possible exception of V_{in}) is always held during the phase when the integrator output is updated. In Appendix A it is shown that this is the condition which must be satisfied for a differencing-input integrator to be equivalent to a single-ended integrator. This means that equations (5.4), (5.5) are valid for the transfer function of the new circuit, with the proviso that the input capacitors (except C_{1b_3}) are divided in value by two.

The input to the third integrator associated with C_{1b_3} is the exception to the above. Since both V_1 and V_3 change on φ_1, if this input is changed to a differencing input, a term $(1-z^{-1})$ will be introduced in the expression for $V_3(z)$. While this will result in a perfectly satisfactory filter, its coefficients will no longer be described by (5.5) and it may be more sensitive to op-amp settling times than that in Fig. 5.7.

It has tacitly been assumed in the above discussion that V_{in} changes only on φ_2. If this is not the case, then the transfer function of the filter, $H(z)=V_o(z)/V_{in}(z)$, must be modified to :

$$H(z) = \frac{0.5\ (1 + z^{-p})\ (a_0 + a_1z^{-1} + a_2z^{-2})}{(1 - b_0z^{-1})\ (b_1 + b_2z^{-1} + b_3z^{-2})} \qquad (5.6)$$

where $p = 0$ if V_{in} changes only on φ_2
where $p = 1$ if V_{in} changes only on φ_1
where $p = \frac{1}{2}$ if V_{in} changes both on φ_2 and φ_1.

These three values of p correspond to the three cases given in Appendix A for the output of a differencing-input integrator.

It follows that, if V_{in} is a continuous-time waveform, or changes at twice the sampling rate of the filter of Fig. 5.7, a cosine filtering/decimation operation is performed on the input. This is implemented in a stray-insensitive circuit, unlike the techniques proposed in [175].

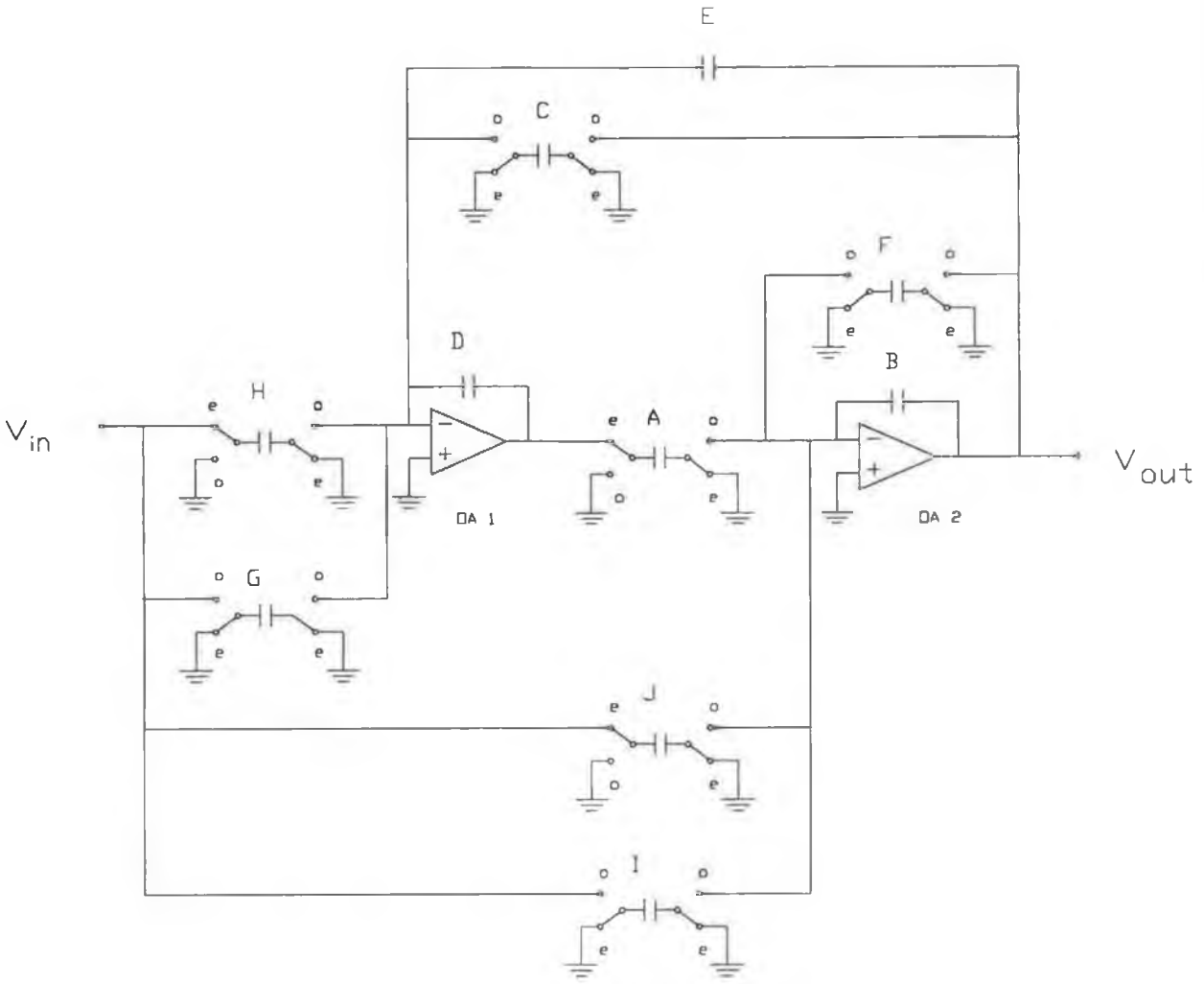


Fig 5.1 The Fleischer-Laker biquad.

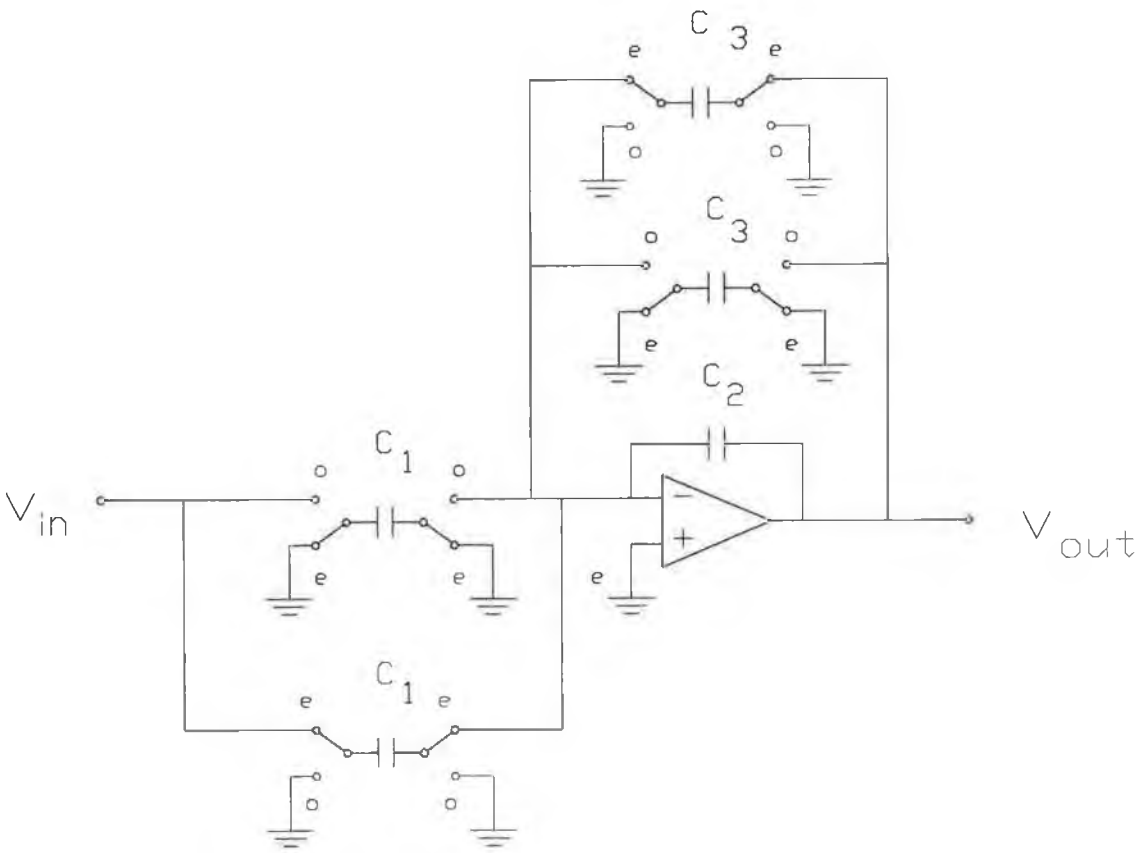


Fig. 5.2: Double-sampling d.d.i.

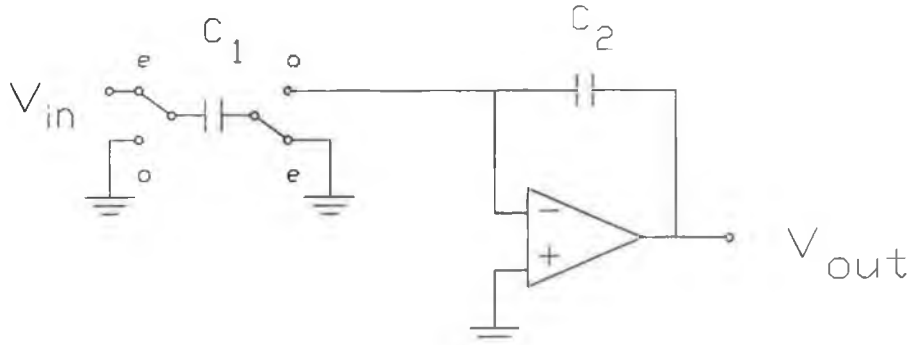


Fig. 5.3(a): single-ended non-inverting l.d.i.

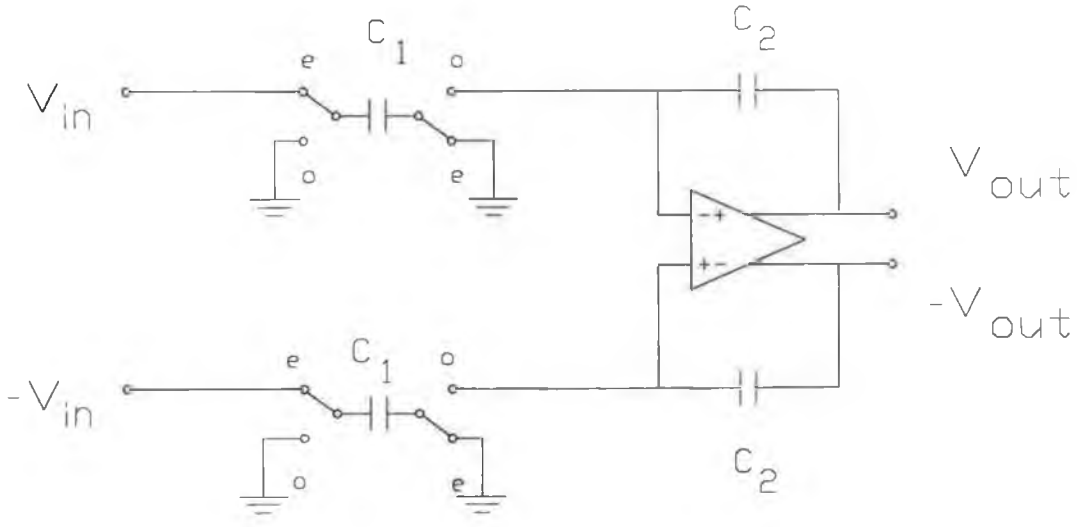


Fig. 5.3(b): Double-ended non-inverting l.d.i.

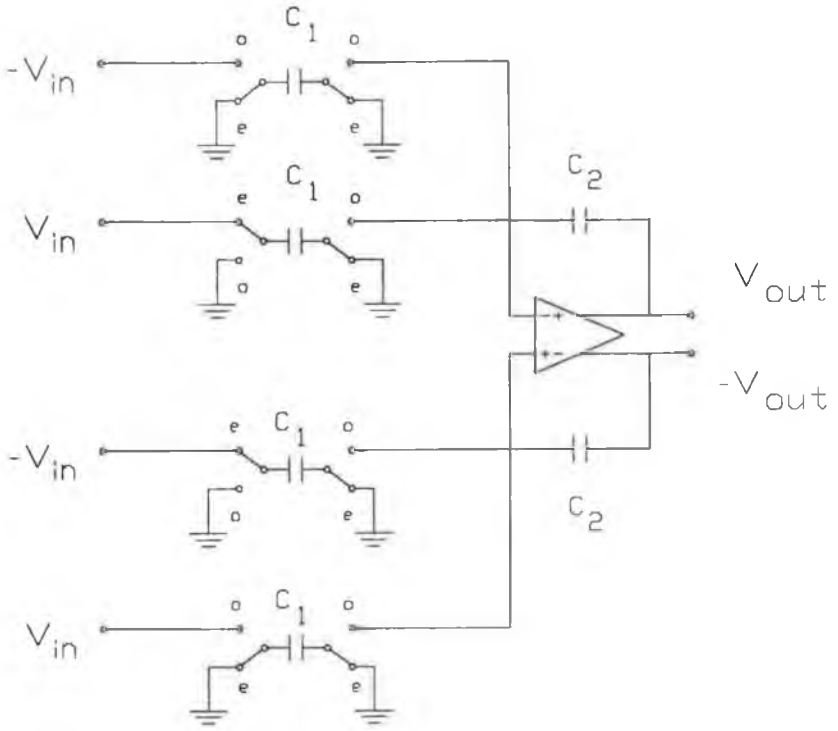


Fig. 5.4: Differencing-input integrator.

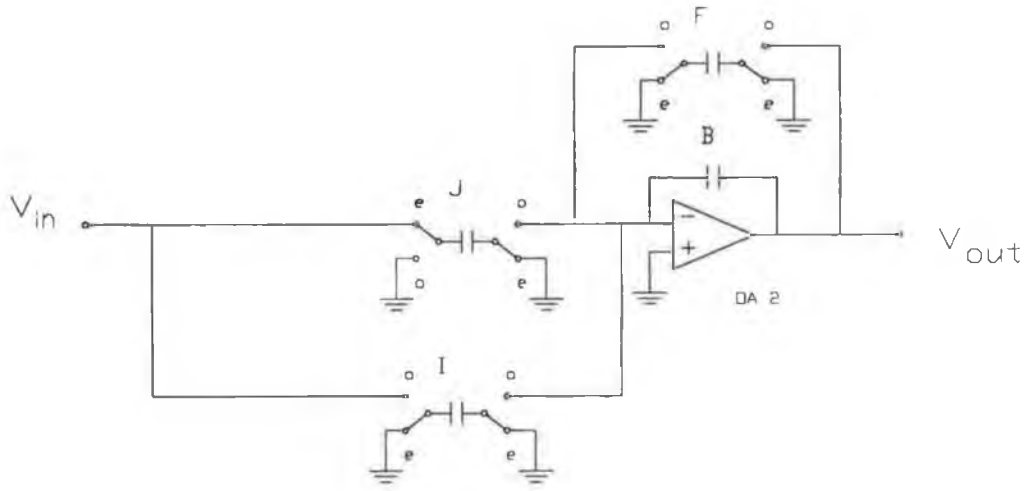


Fig. 5.5: Fleischer-Laker circuit, second stage.

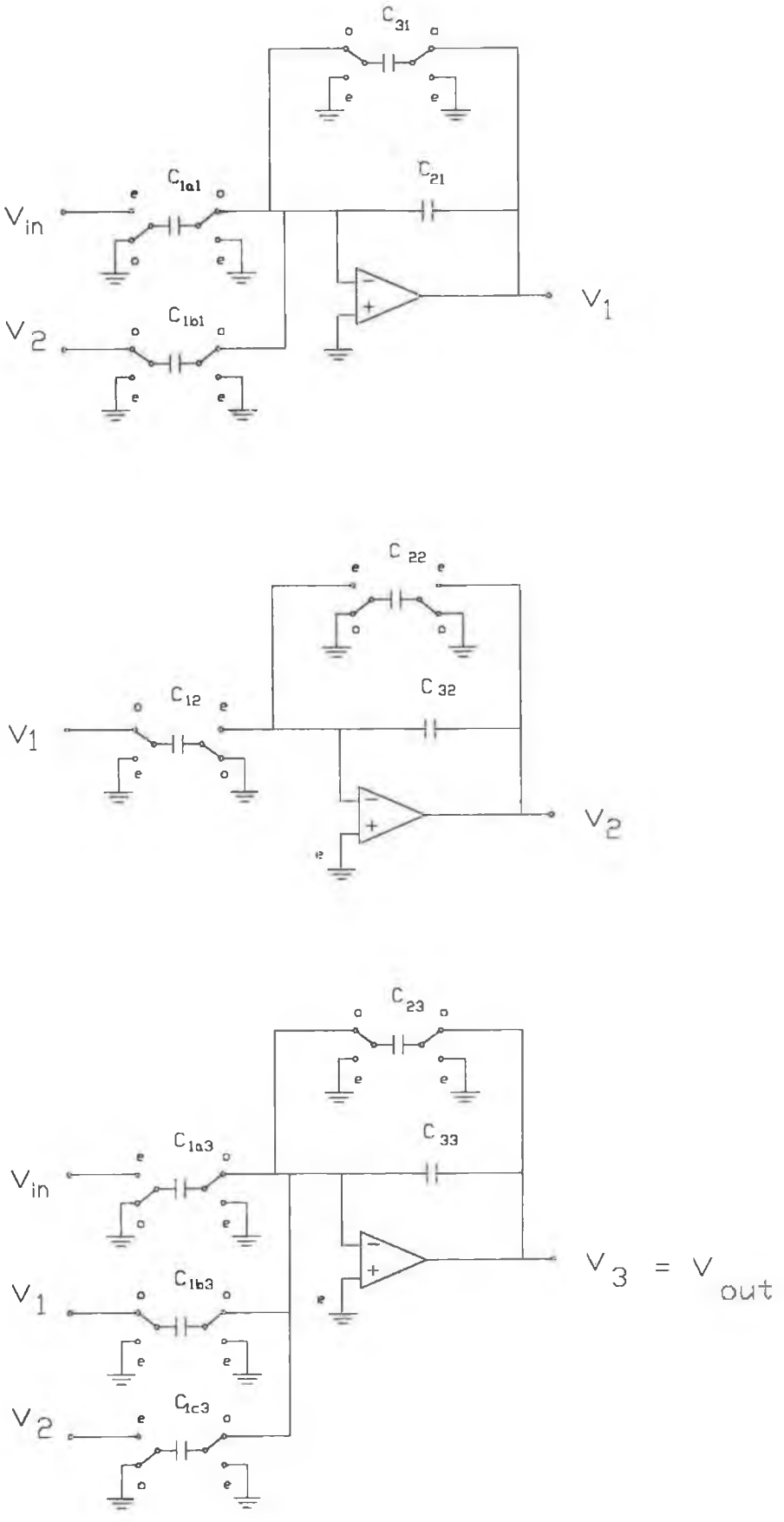


Fig. 5.6: Proposed Filter
Single-ended Version

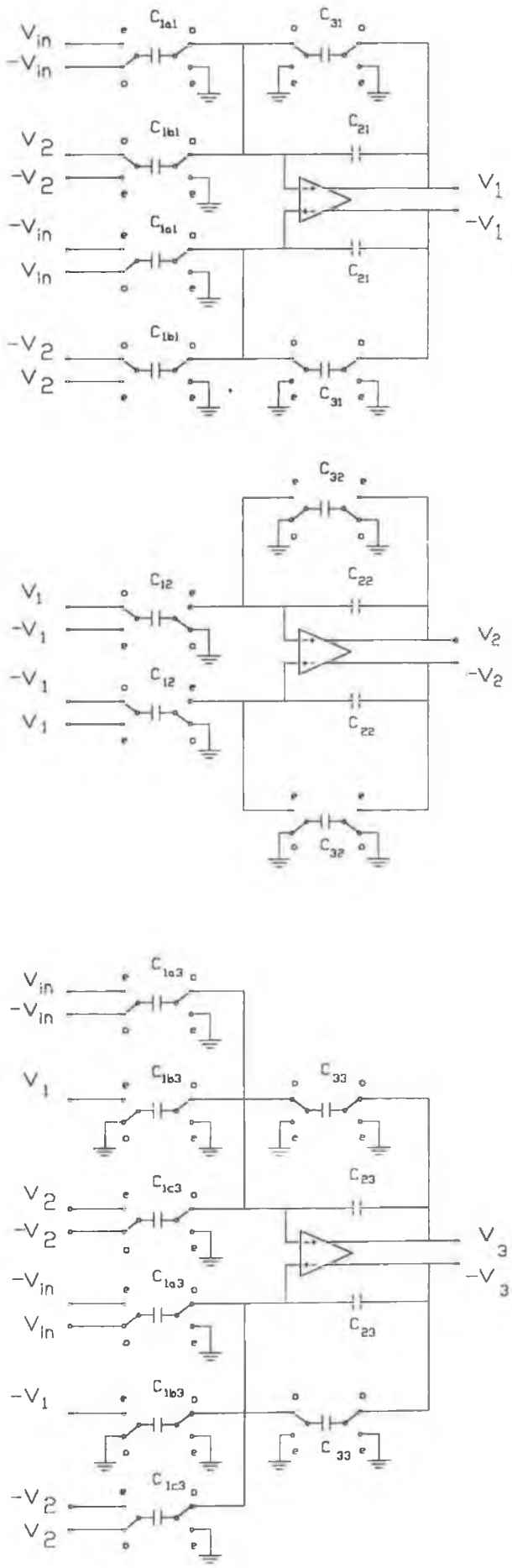


Fig. 5.7: Proposed filter structure - double-ended version.

5.4.4: Synthesis.

5.4.4.1: Constraints on Transfer Function Co-efficients.

The filter design has six parameters (three poles, two zeros and a gain factor) whereas there are twelve capacitor values (nine capacitance ratios). Hence there is some freedom in the choice of capacitor values for implementing a particular transfer function. This freedom can be exploited to maximise the voltage swings at the op-amp outputs or to minimise the total capacitance. For high frequency applications, the most important additional criterion to specify may often be the spread of capacitance ratios.

The equations for the filter coefficients may be rewritten as :

$$
\begin{aligned}
a_0 &= 2ka_3 \ ; \\
a_1 &= a_0 b_2 - 2ka_1(kb_3 + 4kc_3 ka_2) \ ; \\
a_2 &= a_0 b_3 - 2kb_3 ka_1 kd_2 \ ; \\
b_0 &= kd_3 \ ; \\
b_1 &= 1.0 \ ; \\
b_2 &= 4(C_{1b1}/C_{21})(C_{12}/C_{22})b_3 - kd_1 - kd_2 \ ; \\
b_3 &= kd_1 kd_2 \ ;
\end{aligned}
\qquad (5.7)
$$

These equations have been derived from (5.5) but allow for the changes in input capacitor values required for the differencing -inputs. They illustrate how one capacitor value can affect the values of several filter coefficients. Hence it appears that not all possible transfer functions of the form of (5.6) can be implemented. This is because negative capacitors cannot be realised. Thus the pole at $z = b_0$ is constrained to be positive. Also b_1 is unity and b_3 is positive, thereby constraining the remaining two poles to be either both positive, or both negative. The zeros which can be implemented appear to be similarly limited.

Such a conclusion is valid for a single-ended filter design, but a simple topology change allows the double-ended filter to implement a transfer function which, for the original circuit of Fig. 5.7, requires some of the capacitor values to be negative and thus unrealisable. As an example, suppose that the synthesis

yielded negative values for C_{23}, C_{1a3}, and C_{1b3}, using (5.7). Then the circuit of Fig. 5.7 could be used to implement the required transfer function, but with the third integrator modified as shown in Fig. 5.8.

The modification that has been made to this circuit is that, where 'negative' capacitors are required, realisable (i.e. positive) capacitors have been used, but they have been connected to the opposite polarity of input signal. This simple transformation of the circuit topology allows any transfer function of the form of (5.6) to be realised. Thus, for example, the capacitor $|C_{1b3}|$ (where C_{1b3} has been calculated from the required transfer function co-efficients using (5.7), and transpires to be a negative value) in the upper signal path is switched between $-V_1$ and earth, instead of between $+V_1$ and earth as before, and the upper (lower) damping capacitor $|C_{33}|$ is connected to $-V_3$ ($+V_3$) on φ_1 , instead of $+V_3$ ($-V_3$) as before.

The difference equation for Fig. 5.8 is :

$$V_3(n+\tfrac{1}{2}) \tag{5.8}$$

$$= \frac{C_{23}V_3(n-\tfrac{1}{2}) - 2|C_{1a3}|V_{in}(n) - |C_{1b3}|V_1(n) + 2C_{1c3}V_2(n)}{C_{23} - |C_{33}|}$$

$$= \frac{C_{23}V_3(n-\tfrac{1}{2}) + 2\,C_{1a3}\,V_{in}(n) + C_{1b3}\,V_1(n) + 2C_{1c3}V_2(n)}{C_{23} + C_{33}}$$

This difference equation is thus identical to that of the corresponding stage in Fig. 5.7. It follows that where, in the synthesis of the circuit of Fig. 5.7, negative values are obtained for capacitors, these can be replaced by the corresponding positive values, using circuit modifications which introduce signal inversions, (and thus inversions of charge transfers) such as those in Fig. 5.8.

This obviously cannot be done should any of C_{21}, C_{22} or C_{23} be negative, since positive feedback around the associated op-amp would result. However, this situation can always be avoided by, for example, using an algorithm

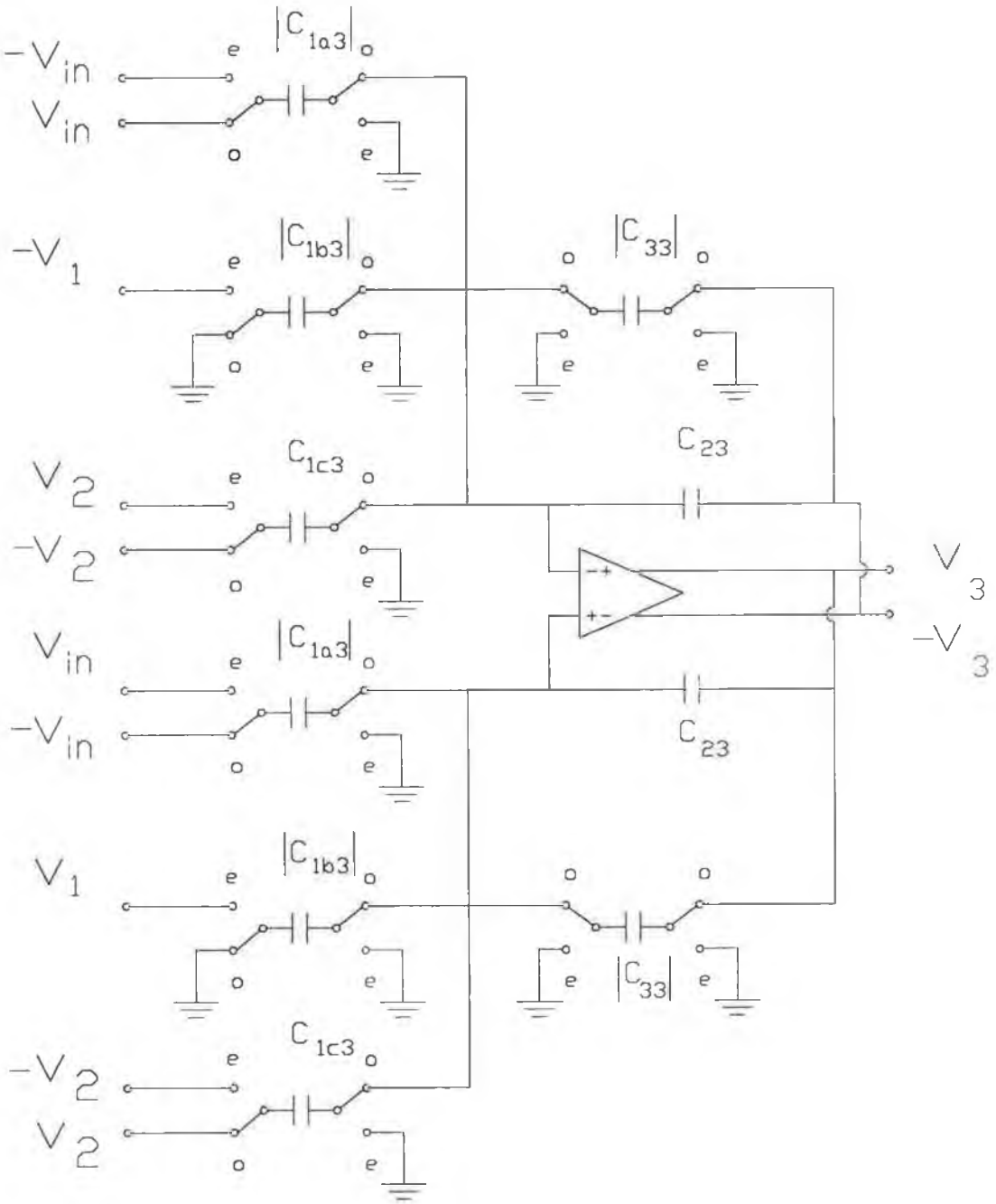


Fig. 5.8: Topological Transformation for maintaining positive capacitor values.

for selecting the capacitor values which, *a priori*, chooses positive values for the feedback capacitors. Thus any stable transfer function of the form of (5.6) can be realised with the circuit of Fig. 5.7, allowing for the possibility of slight topological changes, such as those in Fig. 5.8. Unfortunately, it does not follow that the resulting circuit will feature a low capacitance ratio spread, such as is required for good high frequency performance.

5.4.4.2: Selection of Capacitance Values

A number of approaches could be considered in selecting the capacitor values. One such will now be described. It is assumed that the transfer function coefficients have been obtained in the form of (5.6). Scale the numerator by a factor $k = b_0/a_0$ so that the new a_0 coefficient is equal to b_0. This temporarily reduces the number of degrees of freedom required in the design of the filter to five. Because the number of capacitor values (twelve) exceeds the number of degrees of freedom required, as many as seven of these capacitor values can be arbitrarily chosen. Arbitrarily select $C_{1a_1} = C_{1a_3} = C_{1b_1} = C_{21} = C_{22} = C_{23} = 1.0$. This determines the required values of C_{33} and C_{1b_3} in conjunction with (5.7). Now arbitrarily choose a value for C_{31} (or C_{32}). This determines the value of C_{32}(C_{31}) and could be chosen as zero. The values for C_{12} and C_{1C_3} are now fixed by (5.7).

Where the resulting capacitor values are negative, they can be replaced by positive capacitors using the topological modifications described earlier. The resulting filter produces an output of kV_0 where V_0 is the desired output. To produce the desired output level, the values of C_{23} and C_{33} are multiplied by k.

The filter can also be scaled for maximum dynamic range as follows [18,23]. To increase the voltage V_1 by k without affecting the other circuit nodes, divide the values of C_{21}, C_{31}, and C_{12} by k. Similarly, to increase the voltage V_2 by k, divide the values of C_{22}, C_{32} and C_{1C_3} by k. As a final step, the capacitors for each integrator are scaled so that the smallest is a unit capacitor.

The filter design is now complete. However, in order to achieve the minimum total capacitance, or minimum capacitance ratio spread, the design

procedure should be repeated iteratively for various values of C_{31} (C_{32}) and the realisation which achieves the minimum should be chosen.

5.5 Concluding Remarks.

Some of the limitations of existing SC filter designs when operated over an extended frequency range have been outlined. A new switched- capacitor filter structure featuring fully differential signal paths has been proposed, and has been shown to be capable of implementing any stable function in the z-domain, which has three poles and two zeros, and which features the possibility of cosine filtering and decimation at its input. It remains to investigate practical applications of this new filter structure. This is the subject of the next chapter.

Chapter Six : DESIGN OF A LINE EQUALISER USING SC FILTERING TECHNIQUES

6.1: Techniques for Bidirectional Baseband Digital Communications.

In the previous chapter, a new filter structure for use over an extended frequency range has been proposed. A practical application of this circuit will now be investigated. The intention is that the filter design will be suitable for integration on the 5 μm CMOS process available at the National Micro-electronics Research Centre (the NMRC) in Cork. The chosen application is line equalisation for a digital subscriber (or PABX) loop.

The purpose of such an equalisation system will now very briefly be reviewed. The equaliser is intended for use in a system which allows bidirectional baseband digital communication over two-wire loops, specifically existing subsciber lines (or twisted-pair PABX lines) which are more suited to existing analog telephony signals. Two approaches can be used to this problem.

1) Data can be transmitted in both directions simultaneously. Since both signals occupy the same two-wire loop, inevitably the received signal will be severely contaminated by the locally transmitted signal (i.e. by the so-called echo). A sophisticated adaptive filter, an 'echo canceller ', is used to suppress the unwanted component in the received signal.

2) A half-duplex mode is used, whereby data are transmitted alternately by terminal and exchange, in short bursts, as shown in Fig. 6.1(a). This technique is known variously as burst mode transmission, time compression multiplexing (TCM) or, more colourfully, as 'ping-pong', in honour of the way in which signals periodically alternate in direction.

The second method is technically simpler, at the expense of requiring a channel bandwidth slightly greater than twice that of the first approach. Echo cancellers, with few exceptions [175], are implemented in digital form [e.g. 177-179]. Analog sampled-data forms of implementation are rarely justified, since complex digital control circuitry is required, resulting in an overall circuit complexity approaching that of a wholly digital (i.e. with the exception of an

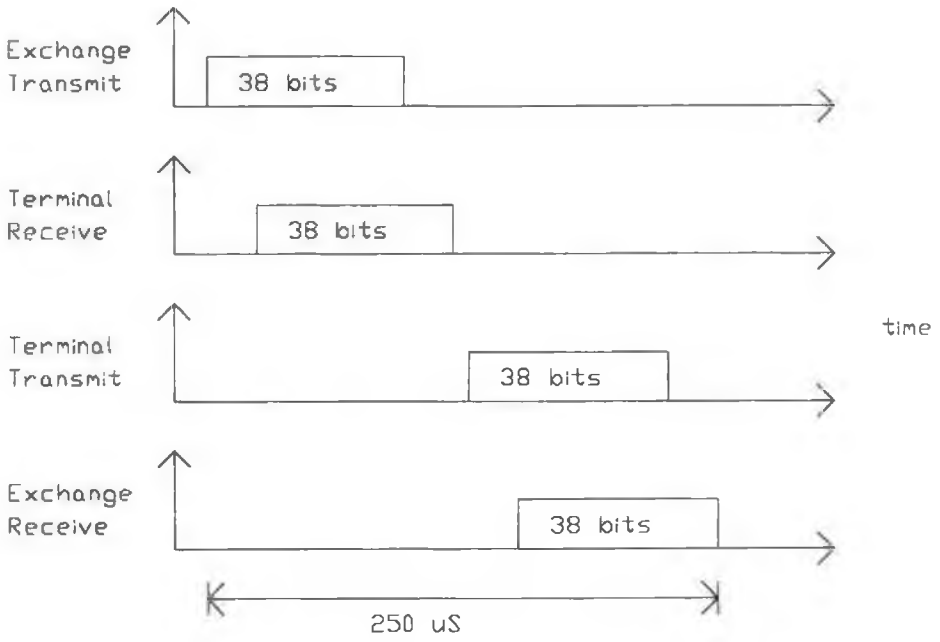


Fig. 6.1(a): Illustration of TCM.

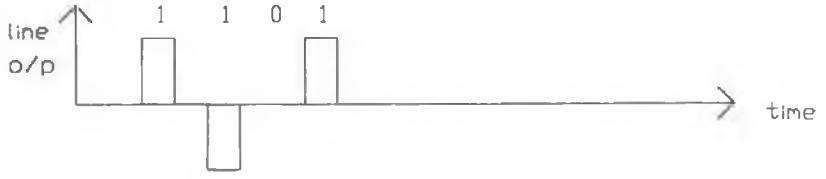


Fig. 6.1(b): An example of AMI.

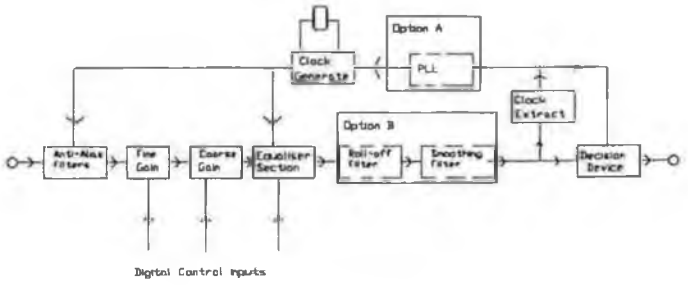


Fig. 6.1(c): SC Equaliser Block Diagram.

ADC) implementation. Switched-capacitor technology is, in any case, inappropriate for this application, since it requires a high signal-to-noise ratio, which is difficult to achieve in switched-capacitor filters [137], and it typically assumes a transversal filter topology, which, while feasible [147], is less suited to switched- capacitor technology than recursive designs based on integrators.

For these reasons, switched- capacitor techniques are best applied to the TCM approach. The principle of TCM is that, whereas the transmit and receive paths are physically the same, they are separated in time. For example, in [155] researchers for Siemens have described how a user bit rate of 144 kb/s, compatible with the requirements for ISDN, could be achieved. Bits are actually transmitted at a rate of 384 kb/s, but are sent in frames of 250 μS duration as follows :

The exchange transmits a burst of thirty eight bits (time taken ≃ 99 μS).
The last such bit is received by the terminal T_d seconds later, where T_d is the group delay of the cable. The Siemens group allowed for $T_{d(max)}$ ≃ 21 μS.
The terminal then waits for a guard time of two bits duration (≃ 2 μS) before switching from receive to transmit.
The above procedure (time taken = 125 μS) is then repeated in the opposite direction.

Thus the cycle repeats every 250 μS, with thirty eight data bits sent and received in each 250 μS frame, as shown in Fig. 6.1(a). This represents an effective bit rate of 152 kb/s. Eight kb/s are used by the system, leaving a user bit rate of 144 kb/s.

The above discussion illustrates the main disadvantage of TCM. In order that an effective bit rate of 144 kb/s be achieved, the channel is required to have sufficient bandwidth to support a bit rate of 384 kb/s. However, the telephone cables used to effect the channel have a frequency response which falls off with increasing frequency. Thus, at the receive end of the channel, a filter is required which will compensate for the frequency distortion introduced by the line, as well as providing Nyquist filtering, to minimise inter-symbol interference [180]. Such a filter is known as a line equaliser.

6.2: A Switched-Capacitor Line Equaliser.

6.2.1: Components of an SC Line Equaliser.

Such an application for SC technology has previously been investigated [149-153,155-157]. The resulting systems can equalise various different line lengths (by implementing various appropriate transfer functions) because programmable capacitor arrays (PCAs) [136] have been substituted for some of the capacitors. Thus they can be digitally programmed. The best choice of the available equaliser transfer functions can be selected, on the basis of the equaliser output, for a particular application. This choice can be made dynamically by adding digital control circuitry which automatically programs the PCAs. This represents a crude form of adaptation, whereby the appropriate equaliser setting is determined by an algorithm implemented by the control circuit. A number of existing designs feature such adaptive algorithms.

The equalisers described above have without exception used a line code of 50% AMI (Alternate Mark Inversion). Thus the symbol '0' is represented by a zero voltage, and the symbol '1' is represented alternately by a positive or negative pulse, whose duration is 50% of the bit interval. This line code, an example of which is shown in Fig. 6.1(b), is simple to implement, but allows the clock signal to be recovered from the received pulses, and has a low d.c. content. These equalisers have been implemented on CMOS processes with feature sizes of 2-3 μm, and use largely standard SC filter circuits, such as the biquad family of Fleischer and Laker [23], and the integrator circuits of [9]. The possibility of using a more conservative process, in conjunction with the newly proposed filter topology, will now be examined.

The minimum requirements of such an equaliser system, as shown in Fig. 6.1(c), are as follows :

1) Programmable gain control.

2) An anti-aliasing filter, to suppress noise and unwanted high frequency components of the signal which would otherwise be aliased into the equaliser passband, because of its sampled-data nature.

3) The equaliser section proper, which can implement a number of transfer functions, as determined by the digital control inputs to the appropriate PCAs. Note

that a distinction is being made between the equaliser *section*, which performs the equalisation, and the equaliser *system*, which includes all the ancillary circuitry necessary for a practical implementation.

4) A decision circuit, which samples the equaliser output at a rate equal to the bit rate, and thereby recovers the data transmitted.

5) Clock extraction circuitry, which provides the clock signals required by the decision circuit and, (assuming synchronous operation of the equaliser, as in [145]) by the switched -capacitor circuitry.

The problem of clock extraction can be a difficult one. However, a digital phase-locked loop has been used for this purpose in [149] and has been successfully integrated. Since such a PLL is not implemented using switched-capacitor technology, its design will not be further discussed here. Similarly, the decision circuit, which can be as simple as a comparator (with a zero voltage reference for the AMI line code) synchronously latched at the bit rate, will receive no further attention. The first three components will now be considered in further detail.

6.2.2: Requirements for the Filtering Stages.

The programmable gain stage could be implemented with either a switched- capacitor gain stage [18] using PCAs or, more conventionally, by a continuous -time amplifier with a tapped resistive divider. The latter approach has been taken for two reasons. A large gain variation in a programmable switched-capacitor gain stage implies a large capacitance ratio spread, which is to be avoided in designs for extended frequency operation. Also, a continuous-time divider can be incorporated in the anti-aliasing filter, reducing op-amp count.

The complexity of the anti-aliasing filter required depends primarily on two factors, the ratio of the equaliser section passband edge (assuming a quasi-lowpass response) to the sampling rate, and the minimum attenuation of aliased signals which will be tolerated in the system. An attenuation of 34-40 dB would ensure that aliased noise would have an amplitude of about 1-2% of its original level, which should be adequate for this application. It remains to determine the system sampling rate.

For this comparatively high frequency application, it is obviously essential that the equaliser sampling rate be as low as possible, since this will reduce the performance requirements for the op-amps and switches, and will result in a reduced capacitance ratio spread. The required sampling rate depends on the equaliser bandwidth. Unfortunately the equaliser section cannot be designed in advance of the anti-aliasing filter, since the effect of the anti- aliasing filter on the equaliser section input signal must be accounted for. Therefore, it is necessary, at this point, to estimate the likely bandwidth of the equaliser section, and to proceed on the basis of that estimate.

The purpose of the equaliser is to minimise inter-symbol interference (ISI). Inter-symbol interference arises due to the dispersal which occurs to a train of pulses as it is passed through a finite-bandwidth channel. At the receiver, the pulse train is sampled at the bit rate. Only one pulse should be present in the received signal when sampling occurs. However, the pulse spreading means that the leading edges of some subsequently transmitted pulses, as well as the trailing edges (typically of much longer duration) of earlier transmitted pulses, contribute to the sampled signal. This can result in the decision circuit producing an erroneous result.

The famous result that the theoretical minimum bandwidth which results in zero ISI is one half of the bit rate is due to Nyquist [180]. For this reason, filters which limit bandwidth while minimising ISI are known as Nyquist filters [181-183]. One transfer function which is frequently used for Nyquist filters is an approximation to the so-called full cosine roll-off (or one hundred per cent raised cosine roll-off) function [184] which ideally blocks all frequencies beyond the bit rate. The equalisers designed in [149-151] all have an amplitude response which rolls off steeply as the bit rate frequency is approached. Consequently, it seems reasonable to assume *a priori*, that the eventual equaliser bandwidth will approximately equal the bit rate.

In the light of this estimated bandwidth requirement, the sampling rate must now be decided. If the equaliser operation is to be synchronised to the bit rate, then this must be an integer multiple of the bit rate. If this synchronism is not incorporated in the system, then the times at which received bits should be sampled by the decision device in Fig. 6.1(c) will not correspond to sampling instants in the equaliser. This means that the equaliser output must be reconstructed

in continuous-time before being applied to the decision device so that it can be sampled at the correct times. The disadvantage of this technique is that it necessitates the use of an additional continuous-time low pass filter (probably in conjunction with a switched-capacitor interpolation filter) which is redundant in a synchronous system, although it does have the advantage that the clock rate for the switched- capacitor filter sections does not track any jitter present in the timing signal extracted from the received pulses, as happens in a synchronous system.

As the sampling rate is lowered, the complexity required of the anti-aliasing filter increases, while the performance required of the op-amps decreases. A sampling rate of four times the bit rate has been adopted in other designs [149-151], and will be similarly adopted here, as it is the lowest practical sampling rate. This means that, since, denoting the bit rate by f_B, the sampling rate f_S is 4 f_B, then the passband of the equaliser will be from approximately zero frequency to 0.25 f_S. Thus the anti-aliasing filter must strongly attenuate any frequency which would be aliased into this frequency range. Since the foldover frequency is at $^1/_2 f_S$, it follows that the anti-aliasing filter must attenuate frequencies in excess of 0.75 f_S by at least 34 dB, the chosen specification.

Whereas the equaliser section itself can be adapted to different bit rates by changing its clock rate, the continuous-time anti-aliasing filter must be designed for a particular cutoff frequency. This necessitates a decision about the required bit rate.

Most of the existing designs assume that the bit rate during the bursts is 200 kb/s [149,150,153]. However, a bit rate of 384 kb/s will be assumed for this design, so as to comply with the standards proposed in [155] for ISDN compatibility. Allowing a passband gain variation of 3dB results in the following specification for the anti-aliasing filter :

Passband		
	Lower edge	zero
	Upper edge	384 kHz
	Maximum attenuation	3 dB
Stopband		
	Lower edge	1.152 MHz
	Upper edge	infinity
	minimum attenuation	34 dB

This tight specification would require a high order filter to implement directly, which, when integrated, is wasteful of die area. One solution to this problem would be to increase the sampling rate, resulting in a corresponding increase in the transition region, and so in a reduction of the required filter order. Instead an equivalent result can be achieved by preceding the equaliser section (with clock rate $f_S = 4f_B$) by another filter with a clock rate of nf_S (n an integer). The continuous- time anti-aliasing filter need now only suppress aliasing associated with the higher sampling rate, and so can be of lower order, while the new filter must suppress frequencies which would otherwise be aliased into the equaliser section passband following the reduction in sampling rate from nf_S to f_S. Such a sampled-data filter is known as a decimator [128].The task of anti-aliasing can thus be shared between the continuous-time section and the decimator.

6.2.3: Filter Circuitry.

6.2.3.1: The SC Low-Pass Filter.

A number of designs have been proposed for SC decimators using polyphase circuits [131,133-134]. However, as well as requiring multiple clock phases, they also pose stringent requirements on op-amp settling time. Thus a conventional l.d.i. based low pass filter structure has been chosen for the decimator, with the exception that it features a fully differential structure, with differencing-input integrators, the benefits of which were described in Chapter Five. The topology of this circuit, which will subsequently be referred to as the SC LPF, and which operates at a clock rate of $2f_S$, is shown in Fig. 6.2(b).

The decimator simulates a simple second order lowpass LC section between resistive terminations [76]. A more selective filter would require either extra op-amps, or additional unswitched capacitors, which would degrade settling times. The low figure for stopband attenuation for this simple circuit is improved somewhat by a feature which is not readily apparent from Fig. 6.2(b). The differential decimator output, which changes at a rate of $2f_S$, will be connected to a differencing-input of the equaliser section, thus providing a cosine filtering action, as explained in Appendix A. Also, because the decimator also features a differencing -input, the continuous-time input signal is effectively sampled at $4f_S$, and is cosine-filtered before a reduction in sampling rate to $2f_S$. The filtering requirements for the continuous-time section can thus be relaxed considerably.

6.2.3.2: Continuous-time Section.

The continuous-time section is shown in Fig. 6.2(a). It must perform the following functions. It must introduce the gain required for the system, since this cannot be done by the SC sections if capacitance ratios are to be kept low. The gain must be programmable. To ease the task of setting the gain, the gain control must consist of a coarse gain and a fine gain adjustment. The continuous-time section must perform an anti-aliasing function, and must convert the single-ended input signal to differential form for the subsequent differential SC sections. Three op-amps are the minimum required to perform these functions. Note that, unlike the corresponding circuit in [155], the filtering action performed is independent of the gain setting (assuming ideal op-amps). The combination of the continuous-time section of Fig. 6.2(a) and the SC LPF of Fig. 6.2(b) is sufficient to meet the required specification for alias rejection.

6.2.3.3: Equaliser Section.

The filter structure proposed in Chapter Five, which is shown in Fig. 6.3, is employed as the basis for the equaliser section. To make the transfer function it implements digitally programmable, a number of the capacitors (the capacitors to be variable to be determined during the design process) must be replaced by programmable capacitor arrays (PCAs). Because PCAs require considerable die area, the minimum number of capacitors possible should be programmable. Fig 6.4 shows how the PCAs are implemented, for the hypothetical

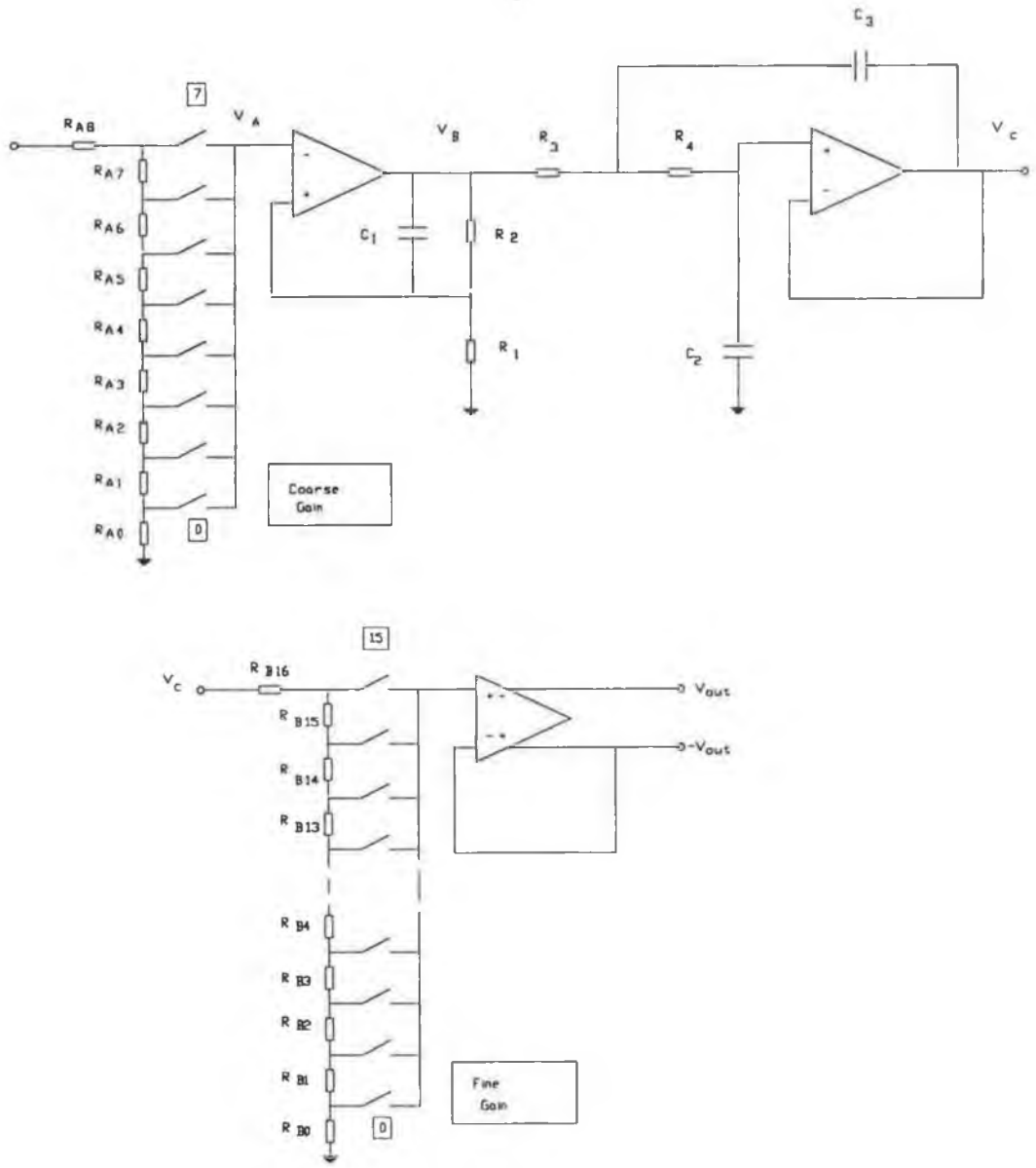


Fig. 6.2(a): Continuous-time Section.

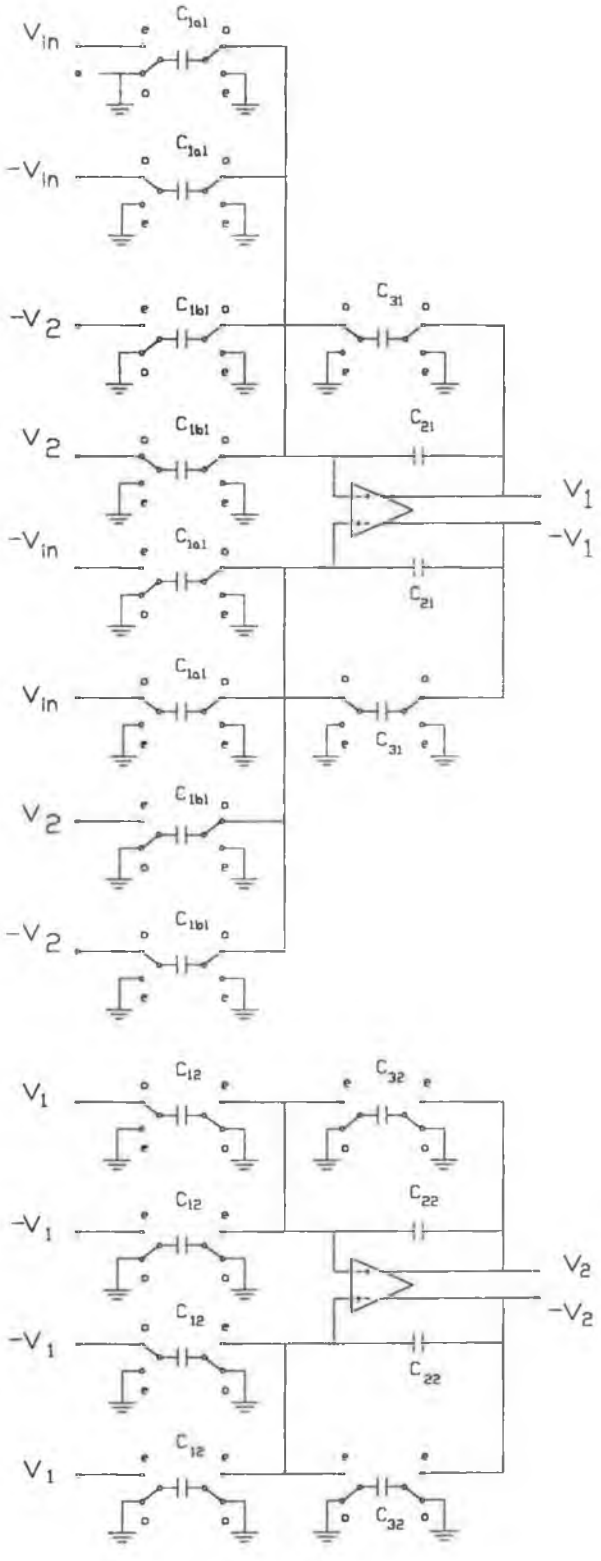


Fig. 6.2(b): SC Low-Pass Filter.

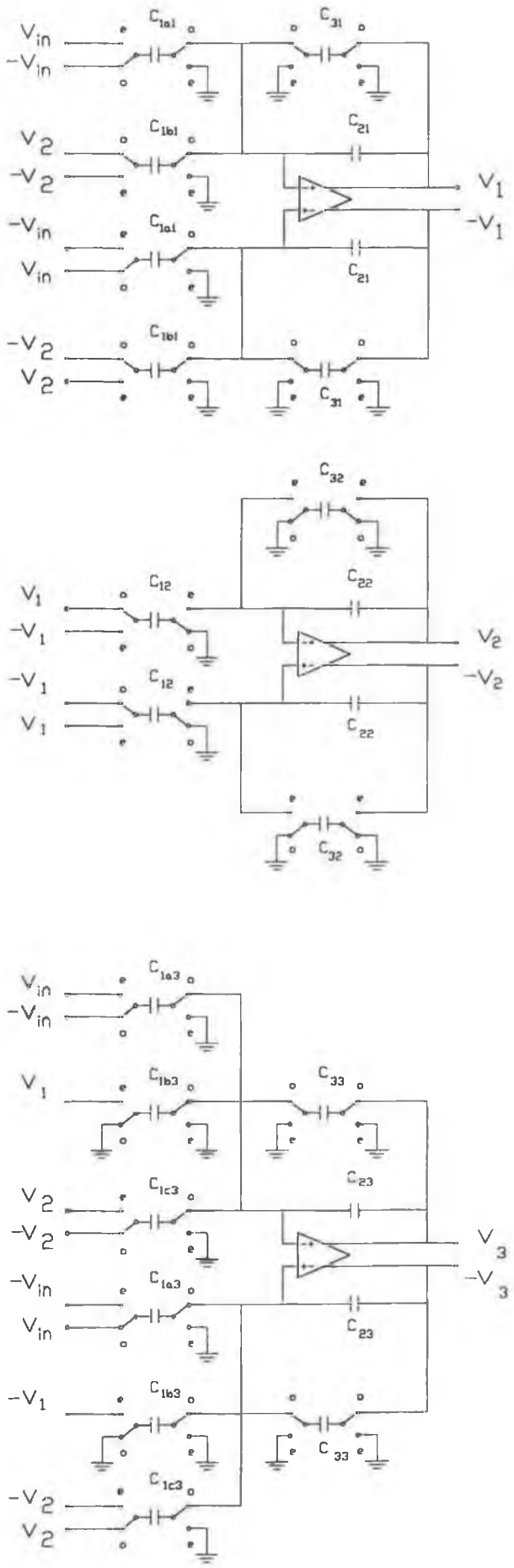


Fig. 6.3: Equaliser Section Structure

situation where C_{22} and C_{12} must be programmable. For any of the PCA settings, only one of the switches shown will be closed. Thus the total capacitance available in the PCA is distributed between the capacitance present in the circuit (between nodes A and B) and the excess capacitance, which is connected (from node A) to earth. Note that this capacitance always appears on the side of the PCA which is (or will be, on the appropriate phase) connected to an op-amp output. This ensures that all the capacitors in the array are precharged to the same voltage as those which are currently in circuit. This reduces the size of the transient which occurs when the effective capacitance is increased by switching in an additional capacitor from the array. Also, connecting the PCA in this sense ensures that the excess capacitance does not appear in parallel with the stray capacitance at the virtual earth point, which would have obvious detrimental effects on circuit performance, even with a nominally stray-insensitive topology.

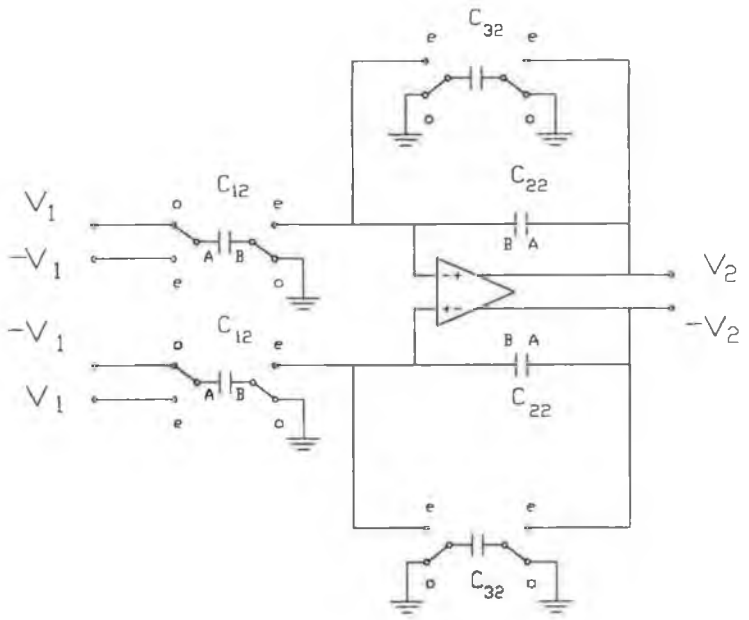
6.3: Element Values for Pre-filter Sections.

The above description gave in qualitative terms the requirements of the equaliser system, and the circuits which have been proposed for implementing these requirements. Quantitative results for the filter transfer function and circuit element values will now be given.

6.3.1: Programmable Gain Stage.

For simplicity in operation, the gain control provided must be monotonic. Thus, for example, the gain with the coarse gain control set to 7 (the maximum gain setting) and the fine gain set to zero (the minimum gain setting) should exceed that with the coarse gain set to six (the second highest gain setting) and the fine gain set to fifteen (the maximum gain setting). To achieve this, the gain variation from one extreme setting to the other of the fine gain control should always be less than the gain variation from one coarse gain control setting to the next. This suggests that, in order to avoid large jumps in gain for low values of the coarse gain, the coarse gain control should follow a power law. Denoting the i-th setting of the coarse gain as CGC_i, this means that

$$CGC_i = k^i \, CGC_0, \quad i = 0,1,\ldots,7 \tag{6.1}$$



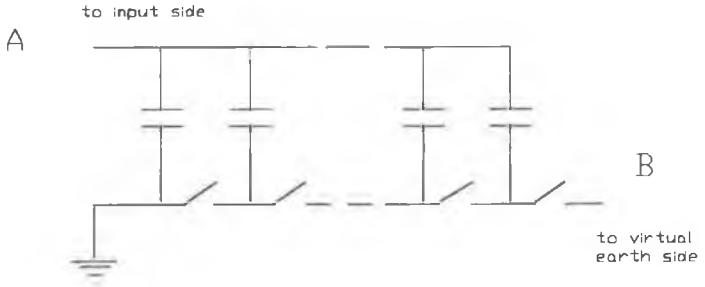


Fig. 6.4: Use of programmable capacitor arrays.

where k is the gain variation from one coarse gain setting to the next. However, the coarse gain is obviously given by

$$CGC_i = \left(\sum_{0}^{i} R_{Aj}\right) / \left(\sum_{0}^{8} R_{Aj}\right) \qquad i = 0,1,\ldots,7 \tag{6.2}$$

Hence

$$CGC_0 = R_{Ao} / \left(\sum_{0}^{8} R_{Aj}\right) \tag{6.3}$$

So

$$CGC_i = \left(\sum_{0}^{i} R_{Aj}\right) CGC_0 / R_{a0}, \quad i=0,1,\ldots,7 \tag{6.4}$$

It follows that

$$k^i R_{A0} = \sum_{0}^{i} R_{Aj}, \quad i=0,1,\ldots 7 \tag{6.5}$$

Thus a recursive formula is obtained for R_{Ai}:

$$\begin{aligned} R_{Ai} &= k^i R_{A0} - \sum_{0}^{i} R_{Aj} \qquad ,i=0,1,\ldots,7 \\ &= (k^i - k^{i-1}) R_{A0} \\ &= k^{i-1}(k-1) R_{A0} \end{aligned} \tag{6.6}$$

The value of k determines the gain variation of the coarse gain control. The maximum variation is equal to

$$CGC_7/CGC_0 = k^7 \tag{6.7}$$

The maximum required gain variation depends on the range of line lengths and types to be catered for by the equaliser system. The achievable gain variation depends on the characteristics of the op-amps used in the implementation, and, in particular, on the unity gain bandwidth, since the op-amps will be required to amplify the signal so as to compensate for the attenuation caused by the resistive voltage dividers. A value of thirty for the gain variation, for typical line types such as 0.4 mm dia. PE or PVC, allows the attenuation of lines up to 1.5-2.0 km in length to be compensated for [155]. For longer line lengths the group delay through the line increases to the point where the guard time between the transmitted and received bursts must be increased, lowering the effective bit rate achievable.

With a maximum gain variation of thirty, the value of k is

$$k = 30^{1/7} = 1.6256$$

R_{A_0} is now arbitrarily set to unity. With this value for k, and using (6.6), the resistor values for the coarse gain control shown in Table 6.1 are obtained. These values must be scaled because the input impedance of the continuous- time section is otherwise very low. The input resistance should preferably be about 10 kΩ, so that the input can be (nominally) matched to a particular line simply by placing an appropriately valued resistor (assuming a purely resistive characteristic impedance for the line) from the equaliser system input (which is the input to the coarse gain control stage) to earth. This resistor might typically have a value in the range 100-300 Ω, which would be loaded negligibly by a 10 kΩ input impedance.

The scaled values for the resistors in Table 6.1 result in a sufficiently high input impedance. The value of R_{A_8} does not affect the gain variation. The chosen value ensures that the attenuation at setting CGC_7 is low. The coarse gain control, as designed, has the following specification :

input resistance	: ≃ 10.1 kΩ
maximum gain	: -0.174 dB
minimum gain	: -29.72 dB
gain steps	: 4.22 dB

Resistor	Value	
	Normalised	Denormalised (Ω)
R_{A_0}	1.00	330
R_{A_1}	0.63	206
R_{A_2}	1.02	336
R_{A_3}	1.65	546
R_{A_4}	2.69	887
R_{A_5}	4.37	1440
R_{A_6}	7.10	2340
R_{A_7}	11.5	3810
R_{A_8}	-	200

Table 6.1 : Coarse gain control resistor values

The above procedure can be repeated for the fine gain control, with the exception that for this stage there are sixteen gain levels and the maximum gain variation is 1.6256, i.e. the value of the incremental gain for the coarse gain control. The resulting resistor values are shown in Table 6.2. In this case, the motivation for scaling is to make the smallest resistor value of sufficient magnitude to be realised with low tolerance on silicon. The values for the fine gain control are not critical, since the main requirement is that the maximum gain variation for the fine gain control should be less than the minimum gain variation for the coarse gain control. This requirement is satisfied if the following constraint holds :

$$\sum_{0}^{15} R_{Bi} < 1.6256\ R_{B_0}$$

Thus, although process tolerances may result in the realised values for R_B

differing considerably from those in the above table, the monotonicity of the gain control is guaranteed if the above criterion is satisfied.

Resistor	Value	
	Normalised	Denormalised (Ω)
R_{B_0}	10.00	5000
R_{B_1}	0.329	165
R_{B_2}	0.340	170
R_{B_3}	0.351	176
R_{B_4}	0.363	181
R_{B_5}	0.375	187
R_{B_6}	0.387	194
R_{B_7}	0.400	200
R_{B_8}	0.413	207
R_{B_9}	0.427	213
$R_{B_{10}}$	0.441	220
$R_{B_{11}}$	0.455	228
$R_{B_{12}}$	0.470	235
$R_{B_{13}}$	0.486	243
$R_{B_{14}}$	0.502	251
$R_{B_{15}}$	0.518	259
$R_{B_{16}}$	-	200

Table 6.2 : Fine Gain Control
resistor values

If the values in Table 6.2 are implemented exactly, then the fine gain control features the following :

maximum gain : -0.21 dB
minimum gain : -4.43 dB
gain steps : 0.28 dB

6.3.2: Continuous-time Pre-filter.

The output from the coarse gain control is connected to the first op-amp in Fig. 6.2(a) which is configured as a non-inverting amplifier with a gain of thirty. This also provides the low-impedance input required by the filter built around the second op-amp. The filter circuit is a standard design frequently used for anti-aliasing applications [175]. After some alternative topologies were considered, this structure was chosen for the reasons which undoubtedly account for its popularity, specifically relatively low (i.e. when compared to other active-RC biquad designs) sensitivity, low element value spread, and element values conducive to integration.

The filter circuit can implement a two-pole filter, which, because of the limited selectivity of the SC LPF of Fig. 6.2(b), does not provide sufficient attenuation. To improve the selectivity, the capacitor C_1 has been added in the feedback path of the first op-amp. It can be easily shown that the resulting transfer function from the input of the first op-amp to its output (assuming ideal elements) is

$$\frac{V_b}{V_a} = \frac{R_1 + R_2 \left(1 + sC_1R_1R_2/(R_1 + R_2) \right)}{R_1 \left(1 + sC_1R_2 \right)} \tag{6.8}$$

The second order filter circuit has the transfer function

$$\frac{V_c}{V_b} = \frac{K \omega_0^2}{s^2 + (\omega_0/Q)\, s + \omega_0^2} \tag{6.9}$$

The minimum sensitivity is obtained with K = 1, which corresponds to $R_3 = R_4 = R$ [185]. In this case the design equations are

$$\omega_0 = 1/(R \sqrt{(C_1C_2)}) \tag{6.10}$$

$$Q = {}^1/_2 \sqrt{(C_1/C_2)}$$

The requirements for the continuous-time filter are:

filter type	: lowpass
approximation used	: third-order Chebyshev (i.e. equiripple passband)
passband ripple 'r'	: 0.2 dB
cutoff frequency	: 384 kHz

The filter should pass all frequencies up to the bit rate. Its transfer function (normalised for a cutoff frequency at $\omega_n = 1$, for $p = j\omega_n$) should be [186]

$$H(p) = \frac{K\eta\,(\eta^2 + {}^3/_4)}{(p + \eta)\,(p^2 + \eta p + \eta^2 + {}^3/_4)} \qquad (6.11)$$

where p is the normalised frequency variable,

$\eta = \sinh({}^1/_3 \sinh^{-1}({}^1/_\varepsilon))$,

$\varepsilon = 10^{\,r/10} - 1$,

and $K = 30$.

The function H(p) can be written as the product of two functions $H_1(p)$ and $H_2(p)$ where

$$H_1(p) = \frac{K\eta}{p + \eta} = \frac{30}{1 + p/0.815} \qquad (6.12)$$

$$H_2(p) = \frac{\eta^2 + {}^3/_4}{p^2 + \eta p + \eta^2 + {}^3/_4} = \frac{1.414}{p^2 + 0.815\,p + 1.414} \qquad (6.13)$$

$H_1(p)$ is implemented by the first filter stage. So

$$(R_1 + R_2)/R_1 = 30 \qquad (6.14)$$

$$C_1R_2 = 1/0.815 \qquad (6.15)$$

$$C_1 \frac{R_1 R_2}{R_1 + R_2} = 0 \qquad (6.16)$$

The third equality (6.16) obviously cannot be satisfied simultaneously with (6.14) and (6.15). Arbitrarily setting $C_1 = 1.0$, from (6.14), (6.15) it follows that

$$R_2 = 1.227$$
$$R_3 = 0.0423$$

Thus an unwanted zero is introduced at p = 24.45 instead of the zero at infinity. The effect of this is to disimprove the filter selectivity in the frequency range above approximately twenty times the cutoff frequency. Since this does not affect the monotonicity of the stop-band attenuation, its effect on filter performance can be neglected.

After frequency scaling for the actual cutoff frequency of 384 kHz, and impedance scaling to obtain element values suitable for integration, the element values are :

$$C_1 = 20.0 \text{ pF}$$
$$R_1 = 877\ \Omega$$
$$R_2 = 25.4\ \text{k}\Omega$$

$H_2(p)$ is implemented by the second stage. This requires

$$\omega_0 = 1.189$$
$$Q = 1.459$$

The value of R is arbitrarily set to unity, so

$$C_2 = 0.288$$
$$C_3 = 2.454$$

After frequency and impedance scaling, the values are

$$R_3 = R_4 = 14.9\ k\Omega$$
$$C_2 = 8.0\ pF$$
$$C_3 = 68.1\ pF$$

The final stage in the continuous-time section is the single-ended to differential conversion. This is simply a fully differential op-amp configured as a voltage follower. Performing this conversion in continuous-time rather than in discrete-time allows the effective sampling rate at the SC LPF input to be doubled.

6.3.3: The SC Low-Pass Filter.

The SC LPF of Fig. 6.2(b) simulates a low-pass ladder in the manner described in [76]. To design this, a single-ended equivalent was first synthesised, using the techniques of Chapter Three, to the following specification:

Filter type	: low pass
Filter approximation	: second-order, equiripple passband
Passband ripple	: 0.2 dB
Clock rate	: 3.072 MHz
Cutoff frequency	: 384 kHz

The values for the double-ended version of this circuit are identical, except that the input capacitor values are divided by two. After scaling the capacitors so that the smallest capacitor is a unit capacitor, the following values are obtained :

$$C_{1a_1} = 1.0$$
$$C_{1b_1} = 1.0$$
$$C_{21} = 3.52$$
$$C_{31} = 2.0$$
$$C_{12} = 1.63$$
$$C_{22} = 1.0$$
$$C_{32} = 2.16$$

Because it is simulating a doubly terminated passive filter, the SC LPF introduces a net loss to the equaliser system. The filter output can be increased in

amplitude by a factor of k by dividing the values of C_{22}, C_{32} and C_{1b1} by k. Since two of these are unit capacitors however, it is in practice necessary to increase the values of C_{1a1}, C_{21}, C_{31} and C_{12} by k instead. This would increase the capacitance ratio for the circuit from 3.52 to 3.52 x k. At the comparatively high operating frequency of this filter, however, a low capacitance ratio spread is paramount in maintaining the filter performance. Thus the signal attenuation introduced by the SC LPF is accepted as the penalty to be paid for achieving the minimum capacitance ratio spread.

Theattenuation of the double-ended SC LPF of Fig. 6.2(b) at frequencies approaching the Nyquist limit is actually greater than that of the single-ended prototype because the SC LPF reads its continuous-time input twice in every sampling period i.e. on both the even and the odd phase. Thus it incorporates a cosine filter at its input. The equaliser section also features such a cosine filter, since its input comes from the SC LPF which operates at twice the sampling frequency. Thus the anti-aliasing function is implemented by four stages of filtering :

1) the third order continuous-time section;
2) the cosine filter at the SC LPF input;
3) the SC LPF itself;
4) the cosine filter at the equaliser section input.

The amplitude response of this combination of filter sections to frequencies in the range 0-16 f_B is shown in Fig. 6.5. This plot has been obtained using the switched- capacitor circuit simulation program SWITCAP [52,53], and can be seen to meet the specification presented earlier for alias rejection, which assumed that the equaliser section rejected signals in the range 384-768 kHz.. The plot shows that signals at frequencies close to the Nyquist limit for the equaliser section, namely 768 kHz, are attenuated by about 20 dB. Thus the equaliser section itself must introduce an attenuation of about 13 dB at 768 kHz, relative to its passband gain, if the specification for alias rejection is to be met by the equaliser system.

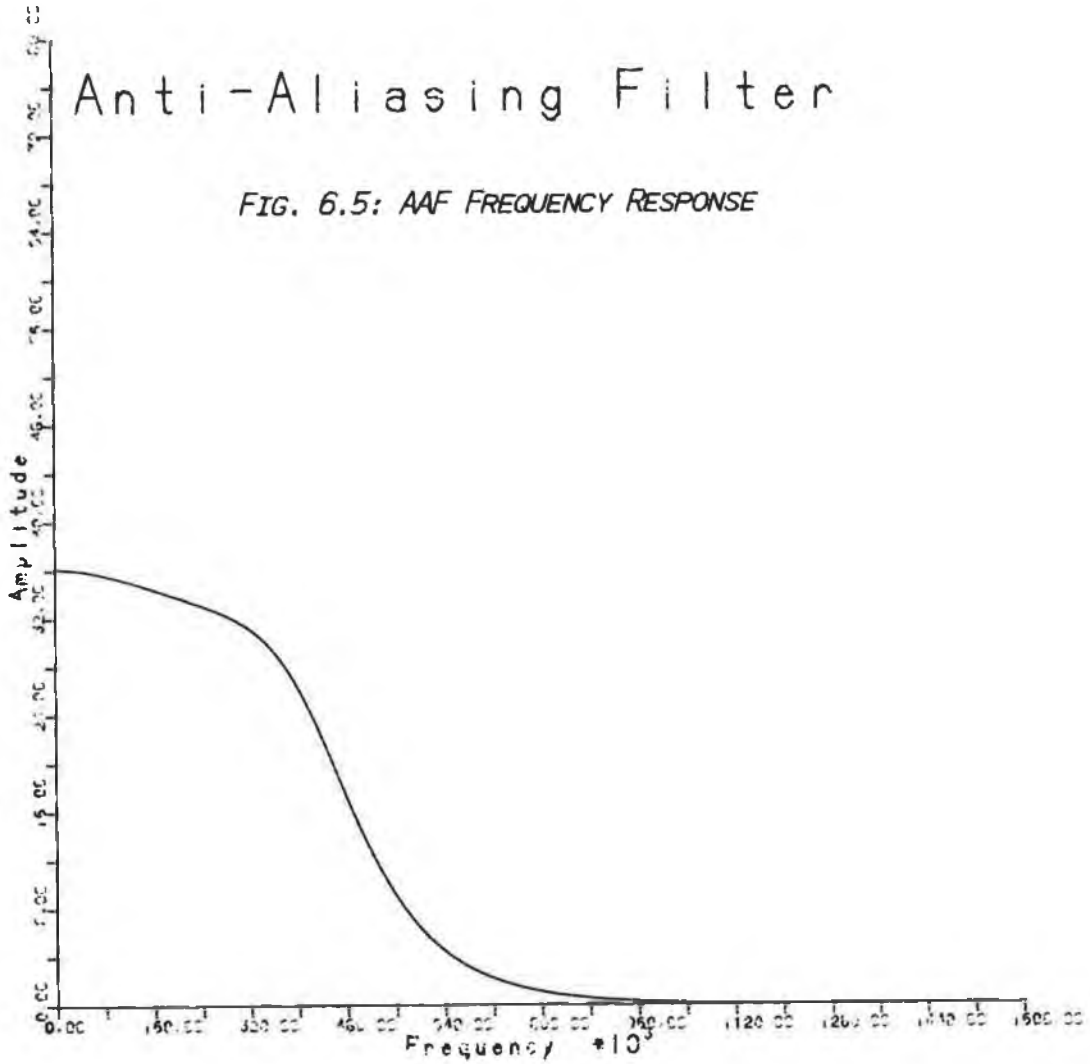


FIG. 6.5: AAF FREQUENCY RESPONSE

6.4: Equaliser Section Design Techniques.

For the design of the equaliser section proper, the signal at the equaliser input must be known. A computer simulation of the response of a transmission line is available at the NIHE, and this is used to generate frequency domain and time domain information about the line response for various line lengths.

Because simple analytical expressions are not available for the line response, it follows that analytical approaches cannot be used for the equaliser section design. An optimisation technique must be used instead, where the function to be minimised (the objective function) in some way measures the departure from ideal operation of the equaliser system. The traditional objective function used in optimising equaliser performance is the intersymbol interference.

The intersymbol interference is defined in the time domain. However, the extended Nyquist criterion [184] provides a frequency domain criterion which results in zero intersymbol interference. Thus the equaliser optimisation can be done in either the time or frequency domains. Both of these distinct approaches are now considered.

6.4.1: Time Domain Optimisation.

6.4.1.1: The Optimisation Method.

The response of the overall system to an isolated pulse of width T/2 (where T is the interval between pulses = $1/f_B$) is considered. The equalised signal g(t) is sampled at the bit rate f_B as shown in Fig. 6.6. The condition for zero intersymbol interference is

$$g(t_d) = A$$
$$g(nT + t_d) = 0 \quad n = \pm 1, \pm 2, \ldots \tag{6.17}$$

where g(t) is at a maximum at time $t = t_d$. Thus the following might be used as an objective function :

$$e = \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} \frac{| g(nT + t_d) |}{| g(t_d) |} \qquad (6.18)$$

Obviously minimising e will reduce the effect of pulse dispersal and so will reduce the bit error rate. This expression must, of course, be modified for use in practice. Thus, in a realisable, causal system, g(t) will be zero for $t < 0$. Also, if the system is stable, linear and time-invariant, and the output possesses no 'd.c. offset', then, for n sufficiently large, $g(nT + t_d)$ will be zero, i.e. the pulse will not be dispersed over an infinite duration. Thus, in practice, the summation need not be done over all possible values of n. To reduce computation time, the value of e can be approximated as

$$\hat{e} = \sum_{\substack{n=n_1 \\ n \neq 0}}^{n_2} \frac{| g(nT + t_d) |}{| g(t_d) |} \qquad (6.19)$$

where the choice of the values of n_1 and n_2 dictates the amount of computing time required.

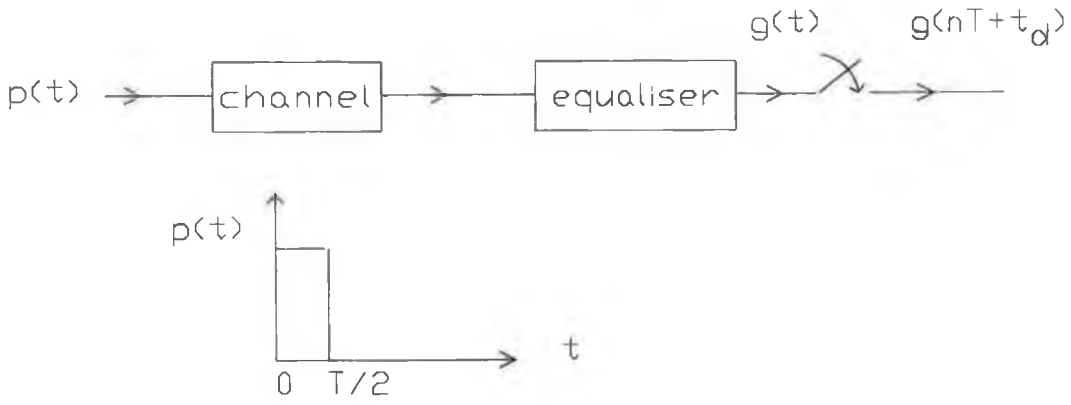


Fig. 6.6: Isolated pulse response.

This approach has been used ,for example, in [151]. One difficulty in the calculation of (6.19) is that the output g(t) must be calculated from t = 0 to $t = t_d + n_2T$. Since the cable group delay increases with increasing line length, the value of t_d increases correspondingly. Thus for different line lengths, g(t) must be calculated for different durations. In practice, this means that g(t) is calculated for a fixed duration or 'window', but for short line lengths the unwanted values of output towards the end of that window are discarded, whilst for long lengths the values for the start of the window are not used. To simplify the calculation of g(t), and to ensure that all calculated values of g(t) are used in (16.9), the expression for intersymbol interference is instead calculated over a fixed window, regardless of line length, from t = 0 to $t = T_W$, where T_W = 65 μS is equivalent to the duration of twenty five bits. This is equivalent to n_1 being the lowest integer such that $n_1T + t_d > 0$, and n_2 being the highest integer such that $n_2T + t_d < T_W$.

6.4.1.2: Practical Considerations.

Thedetails of the algorithm used to perform the time domain optimisation are as follows:

The line simulator is set up to simulate a line type which might typically be met in practice, namely where the line consists of a copper wire pair of diameter 0.4mm, with polyethylene insulation, the line length being selected anew for each optimisation run. The simulator produces an output equivalent to the response of such a line to a pulse of unit amplitude, and of 1.302 μS duration, which is the duration of the pulse representing a mark using the 50% AMI line code, for a bit rate of 384 kHz. The simulation program output represents a sampled-data approximation to the continuous-time output of an actual line. The effective sampling rate is chosen to match the rate at which the SC LPF samples its input, namely 16 x f_B, where f_B is the bit rate 384 kHz. The output consists of 500 samples, representing a duration of 81.4 μS.

The continuous-time filter must be simulated in discrete-time to approximate its response to the line output. A high order rational z-domain transfer function could be used to accurately reproduce the continuous- time response in discrete time. However, because of its simplicity, the bilinear transformation has

been used to map the normalised frequency variable p of (6.11) into the z-domain as follows :

$$p \rightarrow \lambda / \tan \emptyset_0$$

where $\lambda = (1 - z^{-1})/(1 + z^{-1})$ is the bilinear variable, and $\emptyset_0 = \pi f_0/f_S = \pi/16$ is the sampled-data cutoff frequency corresponding to the actual continuous-time filter cutoff frequency $f_0 = f_B$, for a sampling frequency of $f_S = 16\ f_B$. The resulting z-domain transfer function is a close approximation of the original continuous-time function only for frequencies where

$$\tan(\pi\ f/f_S) \cong \pi(f/f_S)$$

Consequently it is a good approximation of the continuous-time filter in the passband, although it exaggerates the filter rolloff in the stopband. Also the unwanted zero at p = 24.45 cannot be mapped accurately into discrete-time by the bilinear transform at the chosen sampling rate, and so it is ignored in the construction of the z-domain transfer function, which is consequently of second order.

The discrete-time transfer function so obtained is implemented in canonical form, its input being the line simulator output. The SC LPF is easily simulated, simply by reproducing in software the difference equations which describe its operation. The SC LPF output in the simulation now contains only 250 samples, because of the decimation introduced by the cosine filter. The signal up to this point is unaffected by the equaliser settings, except for the gain control settings, which do not influence the value for inter-symbol interference, and so can be ignored in the simulation.

After the fixed cosine filter at the equaliser section input has been simulated, the window of calculated signal values contains only 125 sample points. This array of time domain information forms the input for the equaliser optimisation routine. The output of this routine, the objective function to be minimised, is defined by (6.19). The final requirement for the optimisation is a decision as to the parameters to be optimised. Obviously the transfer function must vary with the parameters chosen but a number of possible approaches can be

considered. These include :

1) The capacitor values for the equaliser section can be varied directly.

2) The coefficients of the equaliser section transfer function can be varied, capacitor values which realise this transfer function being selected after the optimisation is concluded.

3) The transfer function poles and zeros for the equaliser section can be varied, capacitor values again being subsequently selected.

Each approach has its own advantages and disadvantages. The first technique allows the capacitors to be determined directly, and so is the most direct. The capacitances can be constrained to ensure a low capacitance ratio spread using constrained optimisation. However the optimisation will terminate prematurely if the capacitor values are such that the equaliser is unstable. Because of the complex relationship between pole locations and capacitor values, the optimisation cannot readily be constrained to keep the transfer function poles inside the unit circle, as required. Also, the equaliser section features twelve capacitor values. Since it features three op-amps, this means that effectively nine capacitance ratios can be varied. To allow all nine ratios to vary would result in an implementation where almost all the capacitors in Fig. 6.3 must be replaced by programmable capacitor arrays. This would require a considerable area on an integrated circuit. Unless the area occupied by the circuit on silicon is not a major consideration (as it must be in any complex integrated system), then it is preferable to fix the values of some of the capacitors. The optimum choices are not immediately apparent, making this approach difficult to apply.

The second approach requires the capacitor values to be determined after optimisation. However, because the co-efficients can be readily expressed in terms of the capacitor ratios and vice versa, this is not a major difficulty. For example, the approach to selecting the capacitor values suggested in Chapter Five can be used. Only five parameters need to be used in the optimisation, since the overall gain does not affect the result of the optimisation. Stability is still not inherently guaranteed, although simple constraints on the transfer function denominator co-efficients [23] will guarantee stability.

The third technique guarantees stability since the poles can simply be constrained to occupy the unit circle. However, a slight loss in flexibility is suffered, in that, for a smooth optimisation to occur, the two zeros and two of the

poles must be restricted to be either complex conjugate, or distinct but real, since the transfer function co-efficients are constrained to be real. This difficulty is not encountered for the second approach, which can smoothly break away from the real axis.

Combinations of the above techniques can also be considered, for example representing the transfer function denominator by its zeros and its numerator by its co-efficients. The pole-zero approach has been adopted for optimising the equaliser design, because of the ease with which stability is assured, and because of the intuitive appeal of the pole-zero approach in designing filters.

One of the optimisation routines available in the IMSL library of mathematical software is used to perform the optimisation [163]. This routine employs a quasi-Newton method to find the local minimum of the (user-written) objective function. It generates its own estimates of the gradient vector and the Hessian matrix. For this application, the objective function performs the following functions:

It calculates the equaliser section transfer function co-efficients from the pole and zero values.

It simulates the equaliser section in software, using a canonical structure, the equaliser input being the time-domain array of samples for the SC LPF output.

It determines the peak sample in the equaliser output. This corresponds to finding the value of t_d in (16.9).

Hence it determines the resulting value of the inter-symbol interference, using (6.19). Because the equaliser section operates at a clock rate equal to four times the bit rate, only every fourth sample of the equaliser output is added to the value for ISI i.e. the value of T in (16.9) corresponds to four samples of the equaliser output.

The value of ISI is returned to the minimisation routine, as the parameter to be optimised.

The optimisation requires an initial guess as to the pole and zero locations. To obtain the global optimum, the optimisation algorithm must be repeatedly applied to a sufficiently wide range of initial sets of poles and zeros to ensure that the global optimum will be recovered. In fact, it is apparent that a

number of different transfer functions could produce the same value for the inter-symbol interference, since the measure of inter-symbol interference is not affected by all the samples of the equaliser output response, but only by one in every four of the samples.

6.4.2: Frequency Domain Optimisation.

6.4.2.1: The Optimisation Method.

The possibility of optimising for minimum inter-symbol interference in the frequency domain arises from the extended Nyquist criterion, which provides a condition on the Fourier Transform of a band-limited pulse waveform which, if satisfied, ensures zero inter-symbol interference for the pulse in the time domain [184].

If p(t) is the time-domain representation of the pulse, and $P(f) = A(f)\, e^{j\Phi(f)}$ is its Fourier Transform (with A(f),Φ(f) both real), then, for a bit rate of f_B, zero inter-symbol interference occurs when :

$$A(\tfrac{1}{2}f_B + f) + A(\tfrac{1}{2}f_B - f) = A(0), \qquad |f| < \tfrac{1}{2}f_B$$

$$A(f) = 0 \qquad |f| > f_B \tag{6.20}$$

with the phase response Φ(f) varying linearly with frequency. This corresponds to a constant group delay, which will not affect the value of inter-symbol interference. It is evident that an equivalent definition is valid in discrete-time.

The optimisation routine must perform the following tasks :

1) Calculate the system pulse response up to the equaliser section input in the frequency domain.
2) Calculate the equaliser section transfer function, and hence the equaliser output, in the frequency range 0 to $\frac{1}{2}f_S$.
3) Determine the magnitude and phase of the equaliser output signal.
4) Measure the extent to which the amplitude response deviates from the criterion in (6.20).

5) Measure the extent to which the phase response departs from linearity.

6) Minimise the departure from the criterion at the equaliser output by using a weighted sum of the above error quantities as the objective function in a minimisation routine.

6.4.2.2: Practical Considerations.

The frequency domain optimisation has much in common with the time domain approach, since the same system is being simulated. Those features which differ from the time-domain method are considered below.

The routines for calculating the outputs of the continuous-time section and the SC LPF must be rewritten so as to produce frequency domain results. One approach is to simply use the FFT algorithm to transform the time domain output of the SC LPF simulation into the frequency domain. Transitions from one domain to the other in this way are likely to cause errors to accumulate, and so are avoided. Instead all calculations are performed in the frequency domain.

This means that a frequency domain output is now required from the line simulation program. The program available could produce only the impulse response (i.e. the transfer function of the line) in the frequency domain, rather than the pulse response required. This must therefore be multiplied by a frequency domain representation of the pulse waveform. The pulse waveform, p(t), in time is shown in Fig. 6.7. The Fourier Transform of p(t) is

$$P(f) = \frac{\sin(\pi/2\ f/f_B)}{\pi\ f} \times e^{-j(\pi/2\ f/f_B)} \qquad (6.21)$$

After sampling at the simulator sampling rate of 16 x f_B, the z-transform of p(t) is

$$P'(z) = 1 + z^{-1} + \ldots\ldots + z^{-7}$$
$$= (1 - z^{-8})/(1 - z^{-1}) \qquad (6.22)$$

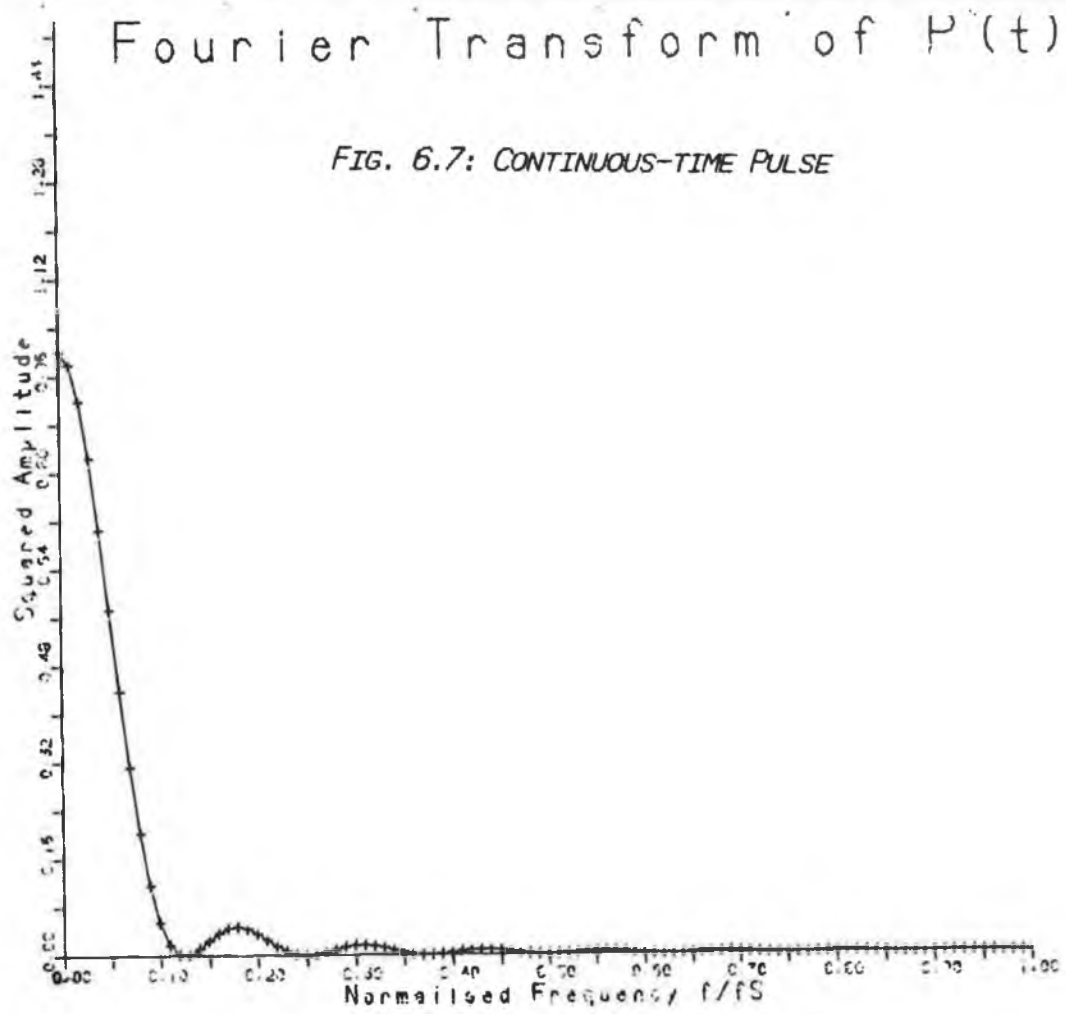


FIG. 6.7: CONTINUOUS-TIME PULSE

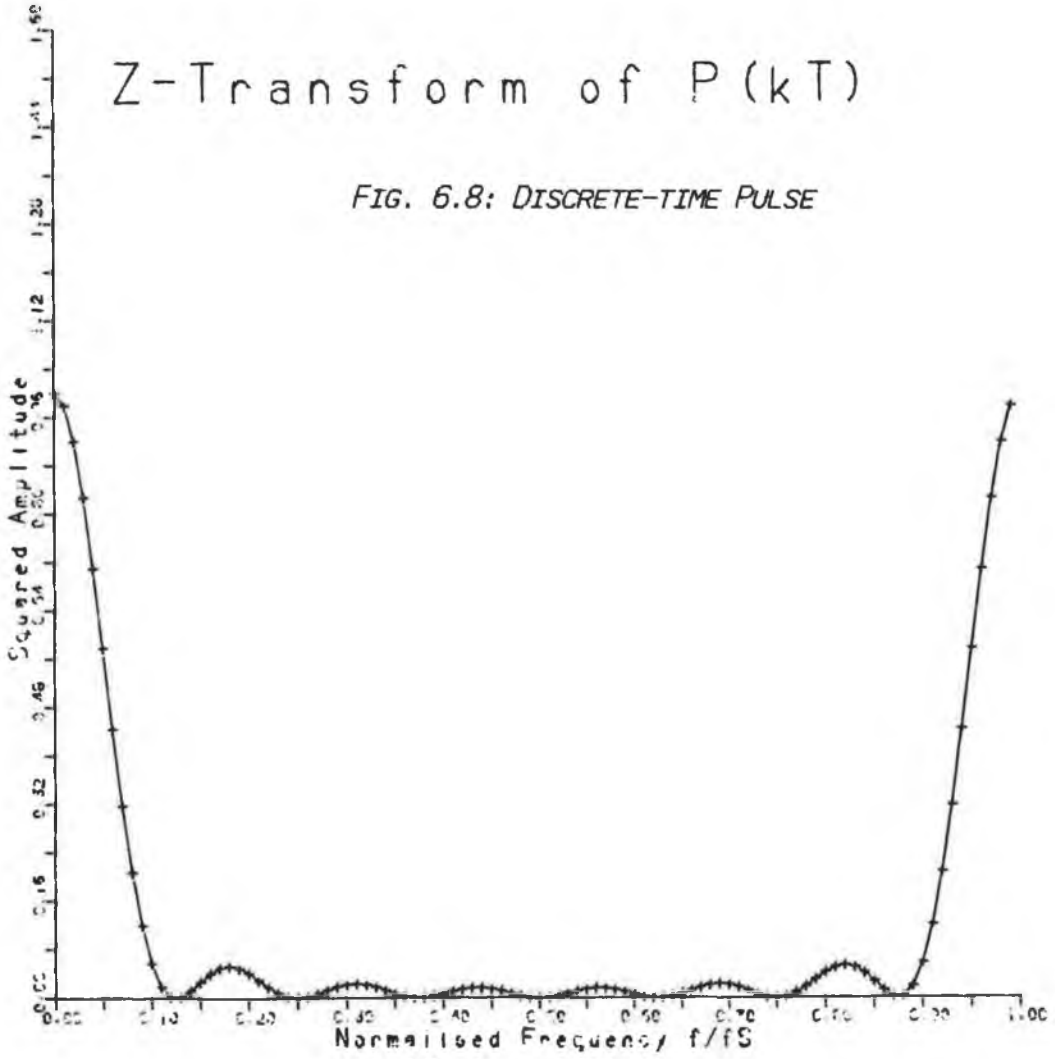


FIG. 6.8: DISCRETE-TIME PULSE

Thus the discrete-time spectrum of the pulse is :

$$P'\left[e^{j(\,2\pi f/f_S)}\right] = \frac{\sin(\pi/2\ f/f_B)}{\sin(\pi/_{16}\ f/f_B)} \times e^{-j(5/_{16}\ f/f_B)}$$

(6.23)

The phase responses in discrete- and continuous- time do not match, but this is not of concern, since both responses vary linearly with frequency. More importantly, the amplitude spectra agree quite closely, as shown in Fig. 6.8. Thus the frequency domain representation of the line pulse response can be found quite accurately by multiplying the frequency response by (6.22).

Another detail which must be considered in the optimisation is the necessity of 'unwrapping' the phase response of the overall system before assessing the phase linearity. The phase of the transfer function, as calculated by the simulation program, will be in the range $-\pi$ to π. Thus, even a transfer function featuring exact phase linearity will appear to be only piecewise linear, because of the effect of the modulo arithmetic used. Unwrapping the phase is achieved by detecting a jump in phase from $-\pi$ to π or vice versa as frequency increases, and by adding the value of $2n\pi$ to the phase at each frequency, where n is the number of complete revolutions from $-\pi$ to π which the phase has traversed from d.c. to the current frequency, as determined by the number of phase discontinuities detected.

After unwrapping the phase response in this way, the departure from phase linearity is determined as follows:

For each frequency, the group delay is estimated as:

$$T_G(f) = \Phi(f)/f \qquad (6.24)$$

where $\Phi(f)$ is the phase response at frequency f (the calculated value is in fact the phase delay, which equals the group delay for a linear-phase response).

The variance of the set of $T_G(f)$ values is determined. For a linear phase response this should be zero. Thus the variance provides a measure of the departure from phase linearity.

One possible error function for use in optimising the amplitude response A(f) is

$$\text{error} = \sum_{|i\Delta f| < \frac{1}{2}f_B} \left(A(\tfrac{1}{2}f_B - i\Delta f) + A(\tfrac{1}{2}f_B + i\Delta f) - A(0) \right)^2 + \sum_{f_B < f < \frac{1}{2}f_S} A^2(f) \qquad (6.25)$$

This error function is zero for a response which exactly satisfies the criterion.

This approach offers no exact control over the frequency response of the system, since various pulses can reduce (6.25) to zero, apart from ensuring that the high frequency gain is minimised. To ensure that the amplitude response is similar in each case when the equaliser is adjusted for various line lengths, which eases the task of selecting an appropriate equaliser setting when it is attached to a line whose length falls between two length settings of the equaliser, a particular amplitude response must be selected which satisfies (6.20) and the equaliser system must be optimised so that the amplitude spectrum of the output pulse approaches that desired.

One family of responses frequently used for this purpose are the raised-cosine responses, first proposed by Nyquist in a classic paper [187], which have the amplitude spectrum (normalised for unity peak gain)

$$A(f) = \begin{cases} 1, & |f| < (1-\rho)f_B/2 \\ \frac{1}{2}\left[1 + \cos\left(\frac{\pi}{2\rho} \left(2|f/f_B| + \rho - 1 \right) \right) \right], & (1-\rho)f_B/2 < |f| < (1+\rho)f_B/2 \\ 0, & |f| > (1+\rho)f_B/2 \end{cases} \qquad (6.26)$$

Here, f_B is the bit rate and ρ is a constant between 0 and 1. With $\rho = 1$, the so-called 100% rolloff raised cosine response is obtained. This has a bandwidth of f_B, and the time-domain response is:

$$p(t) = \frac{\sin(2\pi f_B t)}{2\pi f_B t} \times \frac{1}{1 - 4(f_B t)^2} \qquad (6.27)$$

This response is strictly non-causal, but is negligibly close to zero for $|t| > 3/f_B$. It is thus the easiest of the raised cosine responses to approximate with a low-order filter, featuring as it does the most gradual transition region. Consequently, the 100% raised-cosine response is used in the frequency domain optimisation, as the amplitude response which the overall system should display when a pulse is applied.

The objective function for the optimisation routine must return a weighted sum of the amplitude error and the phase error. The weights are necessary to ensure that the contributions of both amplitude and phase to the objective function result are equivalent, so that the amplitude response is not optimised at the expense of the phase response or vice versa.

As a final check, after the optimisation has been completed, on the validity of the obtained results for the equaliser section transfer function, the pulse response is transformed into the time domain, and the resulting value for inter-symbol interference can be calculated using (6.19).

6.5: Optimisation Results for the Equaliser Section Design.

The results obtained using the two techniques described above are given below.

6.5.1: Time Domain Results.

Results have been obtained using the time domain optimisation technique for four line lengths, 200m, 400m, 600m, and 800m. A line 200m in length displays an acceptably low level of inter-symbol inteference, as determined using the line simulation program, without equalisation, because, even at the proposed bit

rate of 384 kHz, the line is still electrically short. Consequently, applying an optimisation algorithm to a line of 200m length serves to test the validity of that algorithm, since, if it is to produce good results for the longer line lengths which are required in a practical equaliser design, a very low value for inter-symbol interference should be obtained when it is applied to a short line.

The spacing between the lines for which the equaliser optimisation is performed is only 200m. This allows the tradeoff between the range of line lengths catered for in the equaliser design, and the value of inter-symbol interference obtained, to be evaluated. For example, the ISI value obtained when the equaliser is set for a 400m line, while the line length is actually 600m, can be compared to that obtained when the equaliser setting co-incides with the line length of 600m.

As expected from theoretical considerations, a number of local minima are obtained for each line length. A number of observations can be made about the optimisation:

1) In general, convergence is very slow. Typically 250-300 iterations of the optimisation are required before convergence is achieved. The optimisation routine is considered to have converged to a solution when the poles and zeros remain unchanged within a tolerance of 0.1%, this tolerance being less than that likely to prevail on-chip, due to fabrication tolerances on the capacitors.

2) The local minima correspond to a wide range of values for ISI, from very poor figures ($\simeq$ 40%) to very good ones (ISI $<$ 2%).

3) For most initial trial values for the poles and zeros, the value of each pole and zero changes by less than 10%. Thus the choice of initial values is critical in obtaining minima featuring good values for inter-symbol interference.

4) Most of the pole-zero sets which yield good ISI result in unacceptably large capacitor ratios when the equaliser section is synthesised to realise the corresponding transfer function.

It is thus apparent, particularly because of the fourth consideration above, that the necessary approach in designing the equaliser section is not to repeatedly run the optimisation for each line length until the global optimum is found, and then to select capacitor values which will realise the required transfer function. Instead, a number of local minima which result in adequate values for

ISI (the chosen specification being a value for ISI of less than 3% - this is a tighter specification than that chosen by Suzuki *et al.* [149] when allowance is made for the window duration) are listed for each line length. The approach described in Chapter Five for obtaining the capacitor values is applied for each pole-zero set. Many of the sets of poles and zeros prove to result in excessively large capacitance ratio spread, when realised in the form of Fig. 6.3. Many of the remaining sets of poles and zeros, while suitable in themselves for implementation, using the structure of the equaliser section, result in capacitance values which differ substantially for the various equaliser settings. This means that each capacitor in Fig. 6.3 must be replaced by a programmable capacitor array. Since there are twenty four capacitors in all in the equaliser section, the die area required to implement the equaliser section with all capacitor values programmable is prohibitive. Instead the choice of transfer functions must be limited to those which allow common values for some of the capacitors.

This constraint means that deciding upon the transfer functions to be implemented involves choosing, from the lists of poles and zeros for each line length, sets of transfer functions, one for each line length, and, after selecting some of the capacitor values, determining the remaining values for each transfer function using a version of the algorithm suggested in Chapter Five for selecting capacitor values, modified to account for the fixed values of some of the capacitors.

This procedure is repeated until a satisfactory set of equaliser poles and zeros is found. Such a set is shown in Table 6.4, where the equaliser transfer function, neglecting the cosine filter at the input, is:

$$H(z) = \frac{K}{(1 - b_0 z^{-1})} \frac{(1 - a_0 z^{-1})}{(1 - b_1 z^{-1})} \frac{(1 - a_1 z^{-1})}{(1 - b_2 z^{-1})} \qquad (6.28)$$

The value of K is chosen so that the peak magnitude of the equaliser section output pulse is three times that at the equaliser section input. This is sufficient to make up for the losses in the gain control stages at the maximum gain settings, and for the loss of the SC LPF in the passband.

Line length	transfer function co-efficients						
	K	b_0	b_1	b_2	a_0	a_1	ISI
200m	1.470	0.624	-0.409	-0.229	3.21	0.960	2.40×10^{-2}
400m	0.953	0.578	-0.168	-0.361	4.73	0.875	2.51×10^{-2}
600m	1.131	0.552	-0.179	-0.347	0.808	4.750	2.67×10^{-2}
800m	3.578	0.500	-0.309	-0.362	0.778	1.922	2.86×10^{-2}

Table 6.3 : Transfer function co-efficients for various equaliser settings

Note that b_0 has been constrained to be greater than 0.5. For the pole-zero settings of Table 6.3, it is found that fixing the following capacitor values results in reasonable values for all other capacitors, for all equaliser settings :

$C_{21} = 1.0$
$C_{12} = 1.5$
$C_{22} = 2.0$
$C_{32} = 4.0$
$C_{33} = 1.0$

Then the remaining capacitor values are as shown in Table 6.4.

Capacitor	Line length			
	200m	400m	600m	800m
C_{1a_1}	9.79	11.0	10.7	7.72
C_{1b_1}	4.46	5.74	5.61	4.06
C_{31}	2.56	4.50	4.37	2.09
C_{1a_3}	1.95	1.13	1.26	3.58
C_{1b_3}	-6.37	-6.91	-7.14	-5.90
C_{1c_3}	2.95	3.45	3.31	1.12
C_{23}	1.66	1.37	1.23	1.00

Table 6.4 : Equaliser section capacitor values.

The values obtained for C_{1b_3} are negative. Thus, the circuit of Fig. 6.3 must be transformed as explained in Chapter Five, by modifying the third stage so that the inputs from $\pm V_1$ connected to the capacitors listed as C_{1b_3} have the opposite polarity to that shown in Fig. 6.3. Then, for example, the value of C_{1b_3} used for the 200m line setting will be 6.37. Note the low capacitance spread of the filter, 12:1. This is a result of the rejection of transfer functions which resulted in low values for ISI, but a large capacitance ratio spread, and an optimisation of the circuit for mimimum capacitance ratio spread, using the single degree of freedom available, given that the values of five of the capacitors are fixed.

Fig. 6.9 shows the pulse response at the line output for each line length. Fig. 6.10 shows the response at the equaliser section output, for each line length, with the equaliser at the setting appropriate to that line length. Fig. 6.11 shows the amplitude frequency response of the equaliser section alone, for each setting, as determined using the switched-capacitor simulation program SWITCAP.

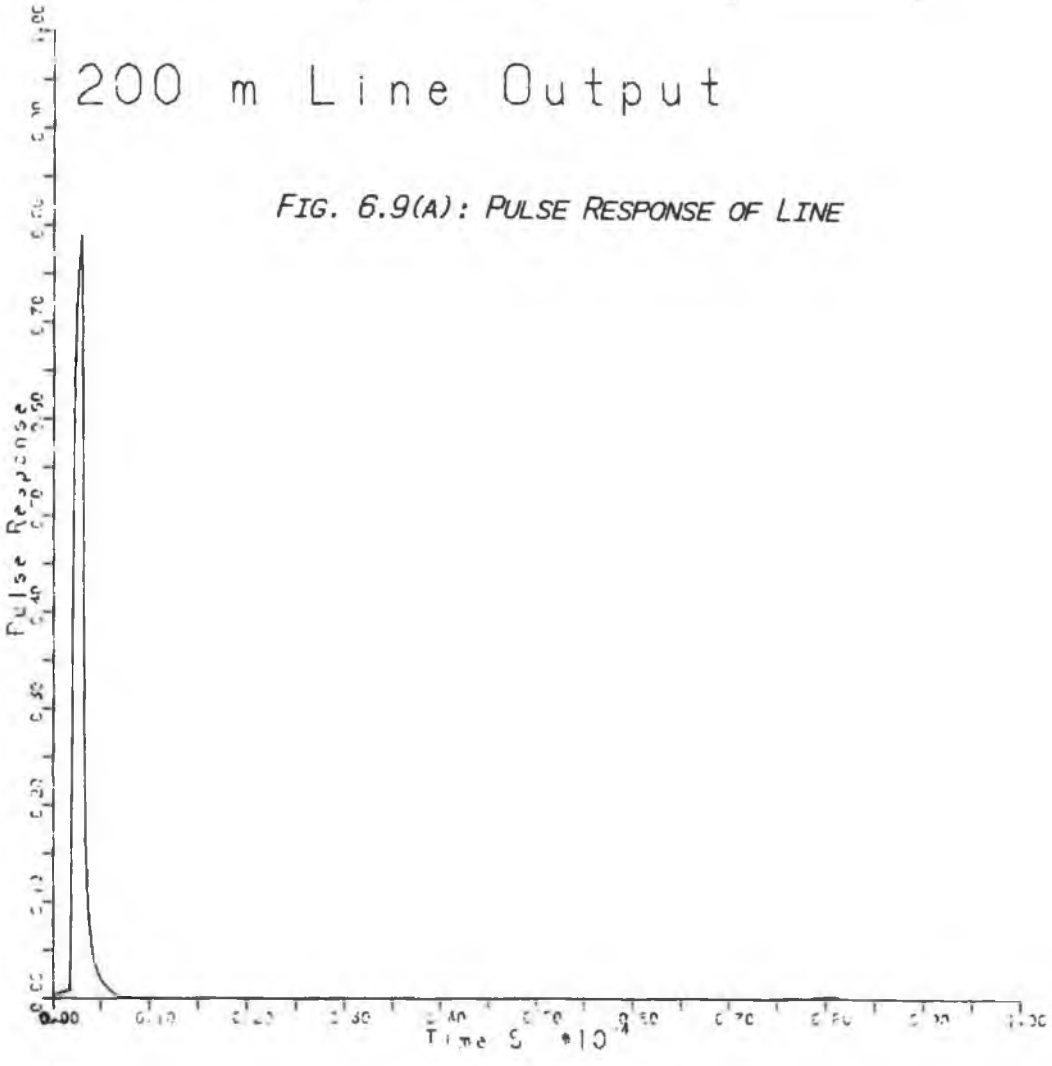


FIG. 6.9(A): PULSE RESPONSE OF LINE

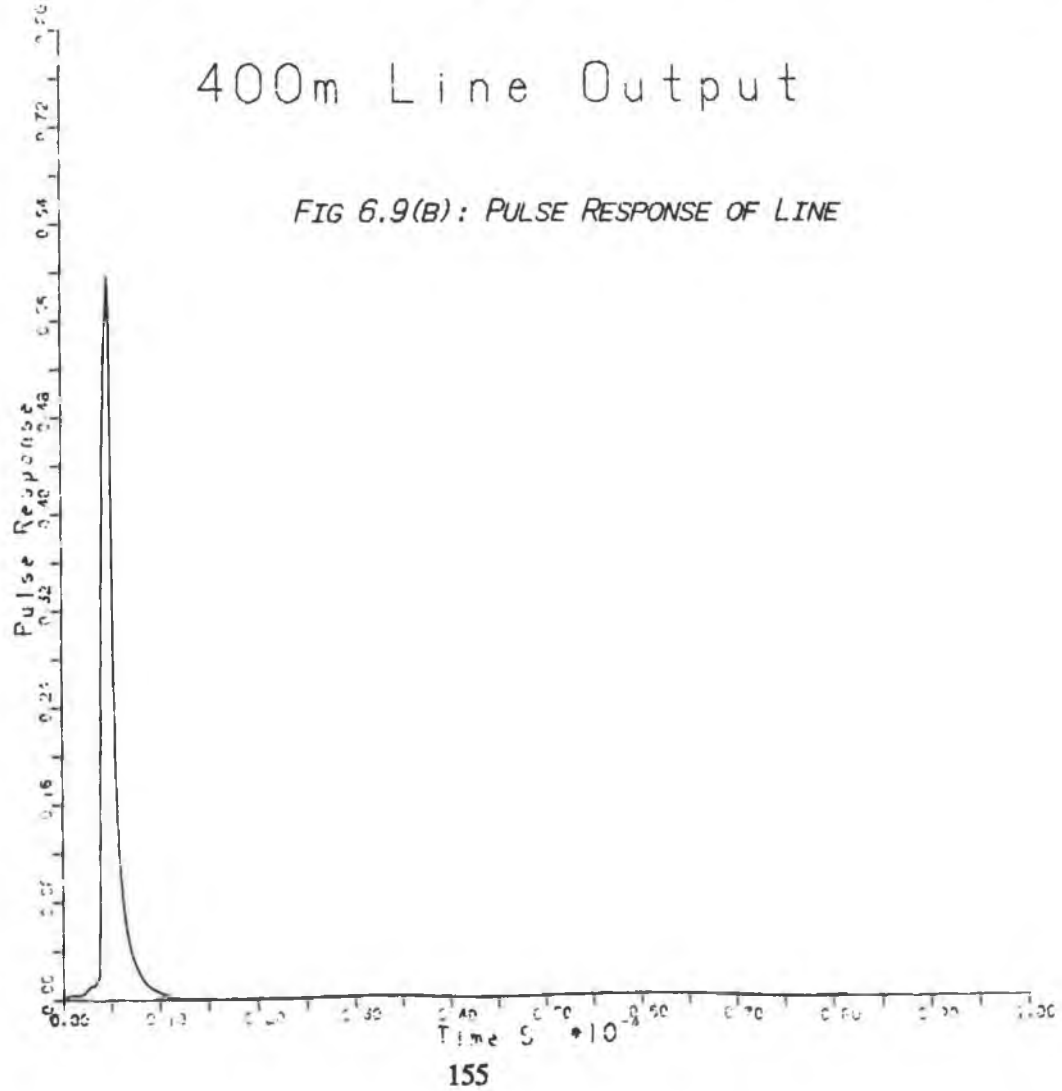


FIG 6.9(B): PULSE RESPONSE OF LINE

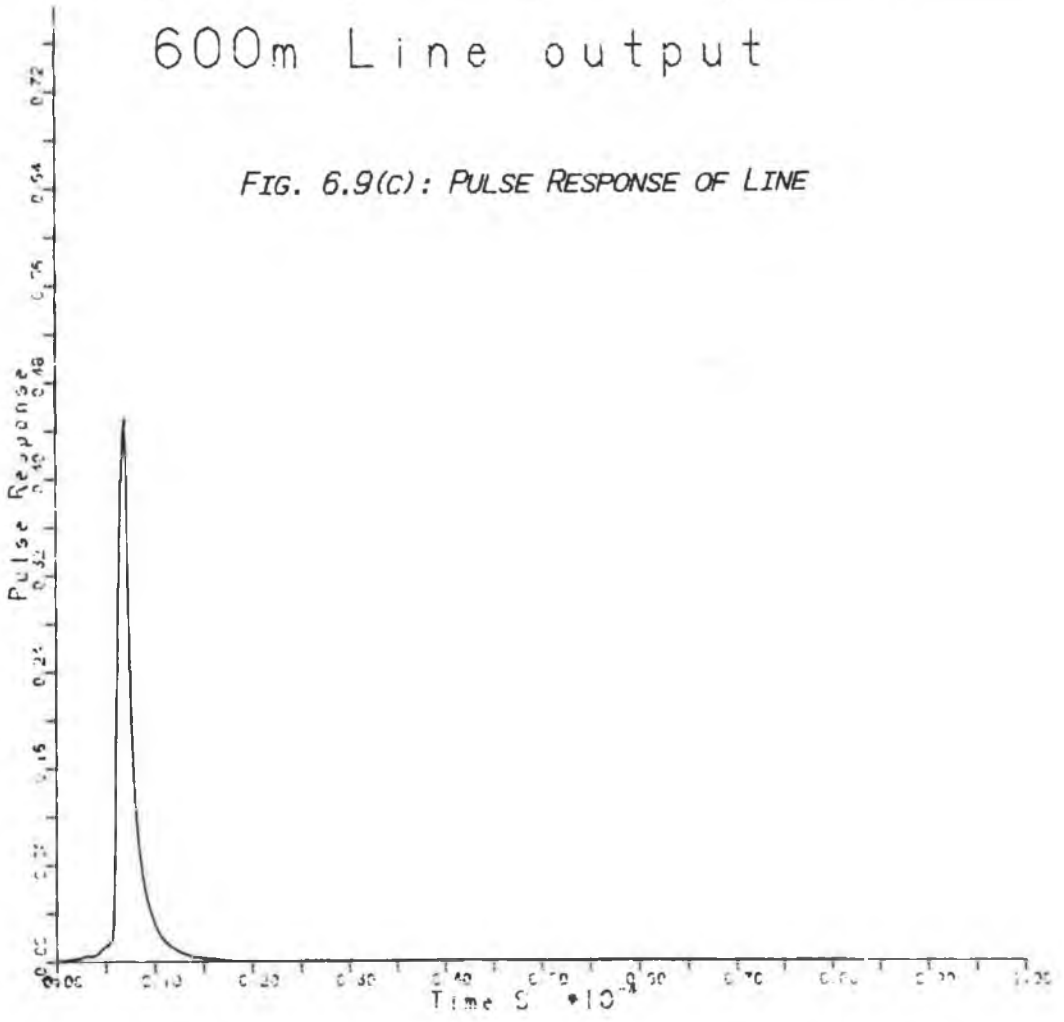


FIG. 6.9(C): PULSE RESPONSE OF LINE

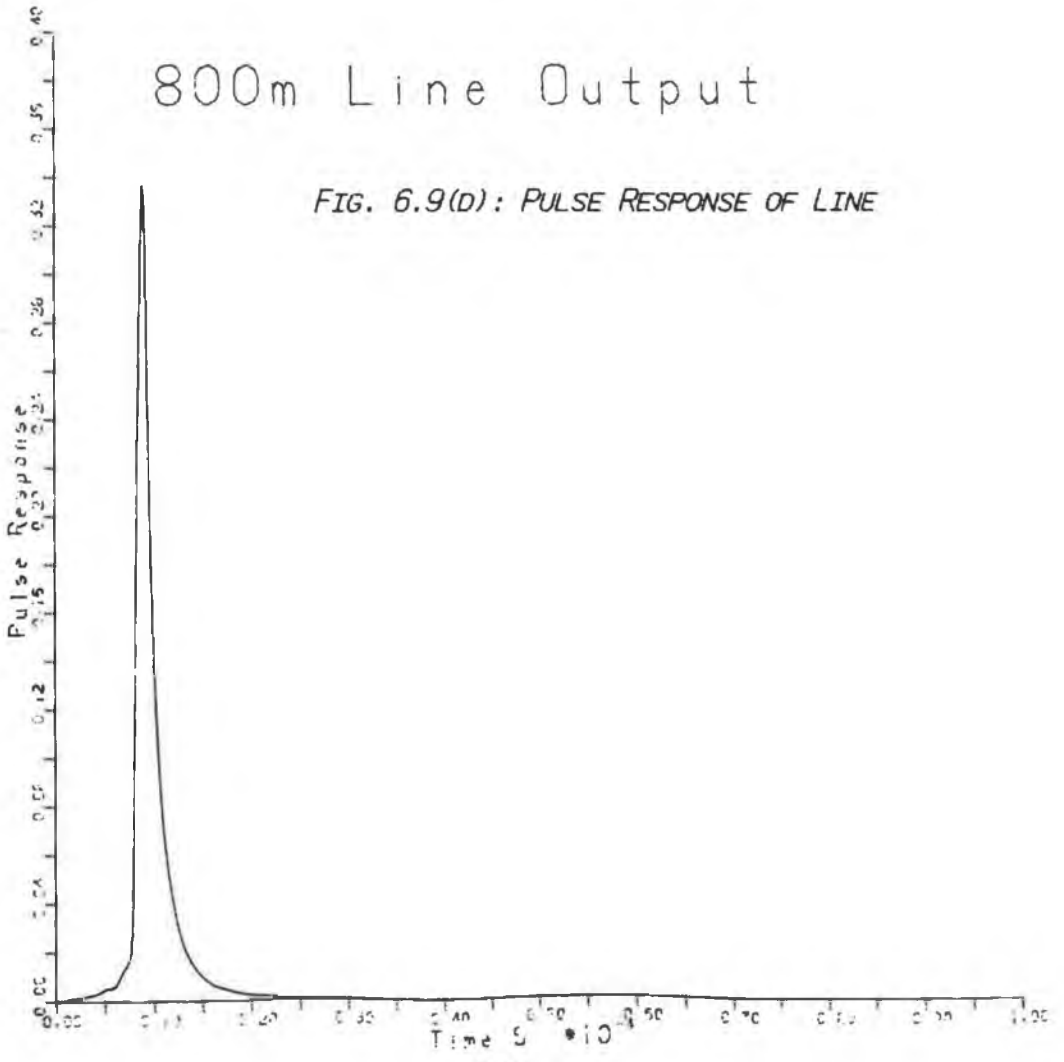


FIG. 6.9(D): PULSE RESPONSE OF LINE

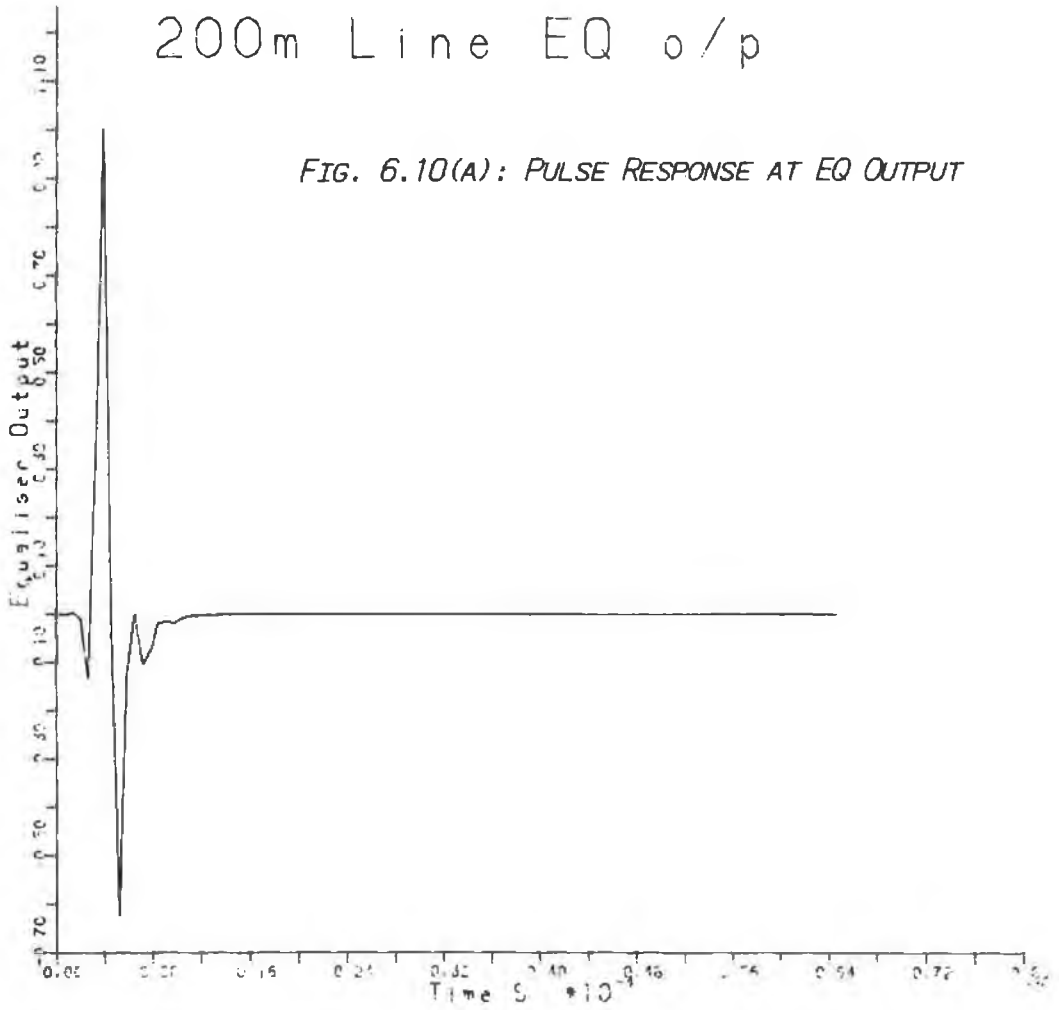


FIG. 6.10(A): PULSE RESPONSE AT EQ OUTPUT

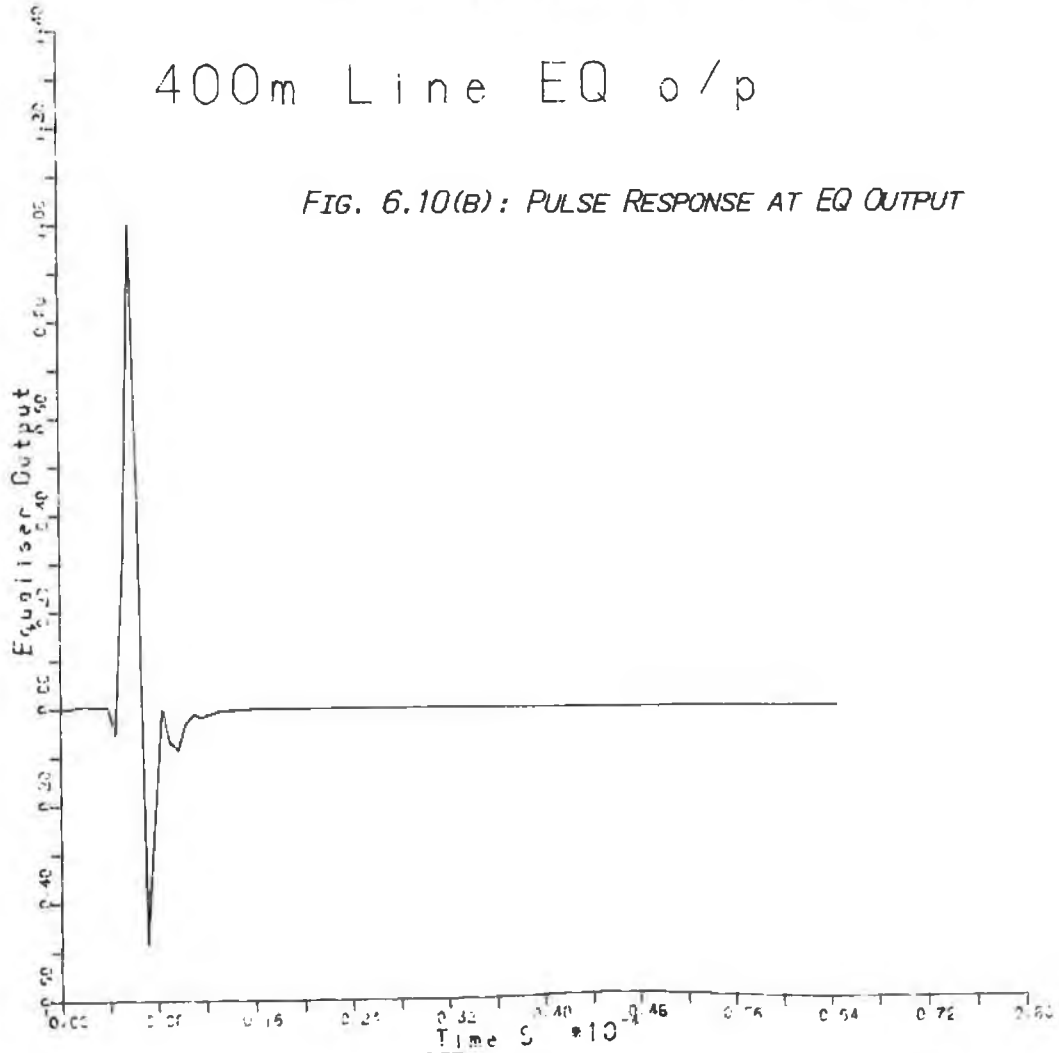


FIG. 6.10(B): PULSE RESPONSE AT EQ OUTPUT

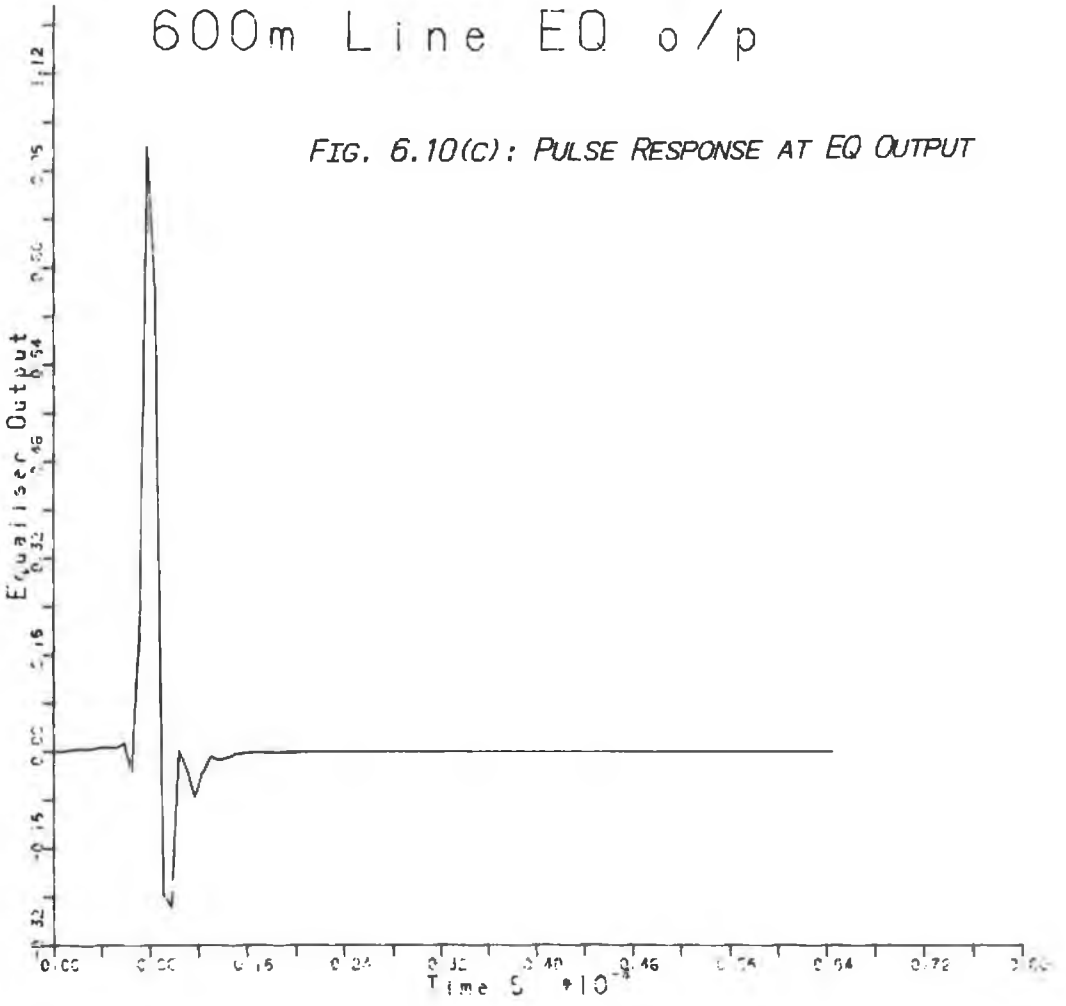


FIG. 6.10(C): PULSE RESPONSE AT EQ OUTPUT

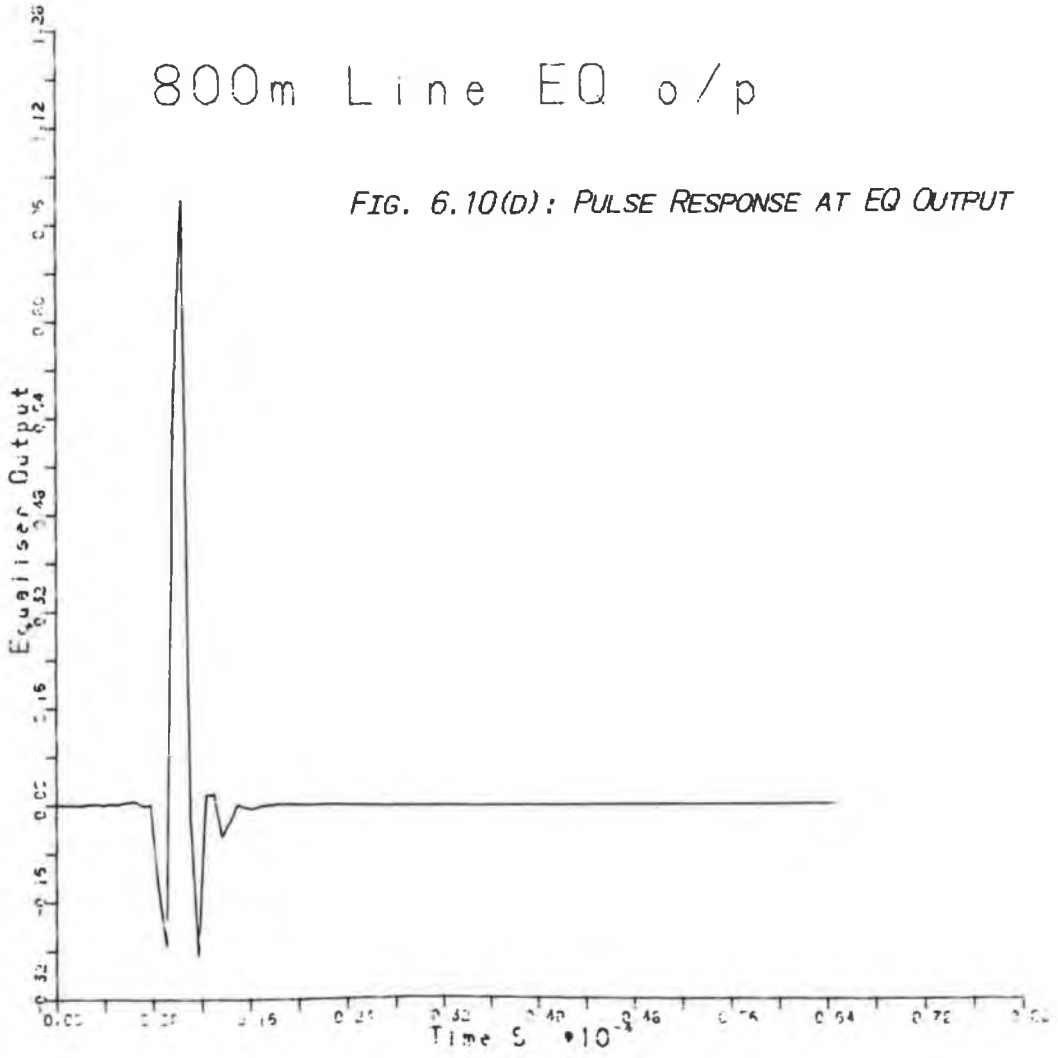


FIG. 6.10(D): PULSE RESPONSE AT EQ OUTPUT

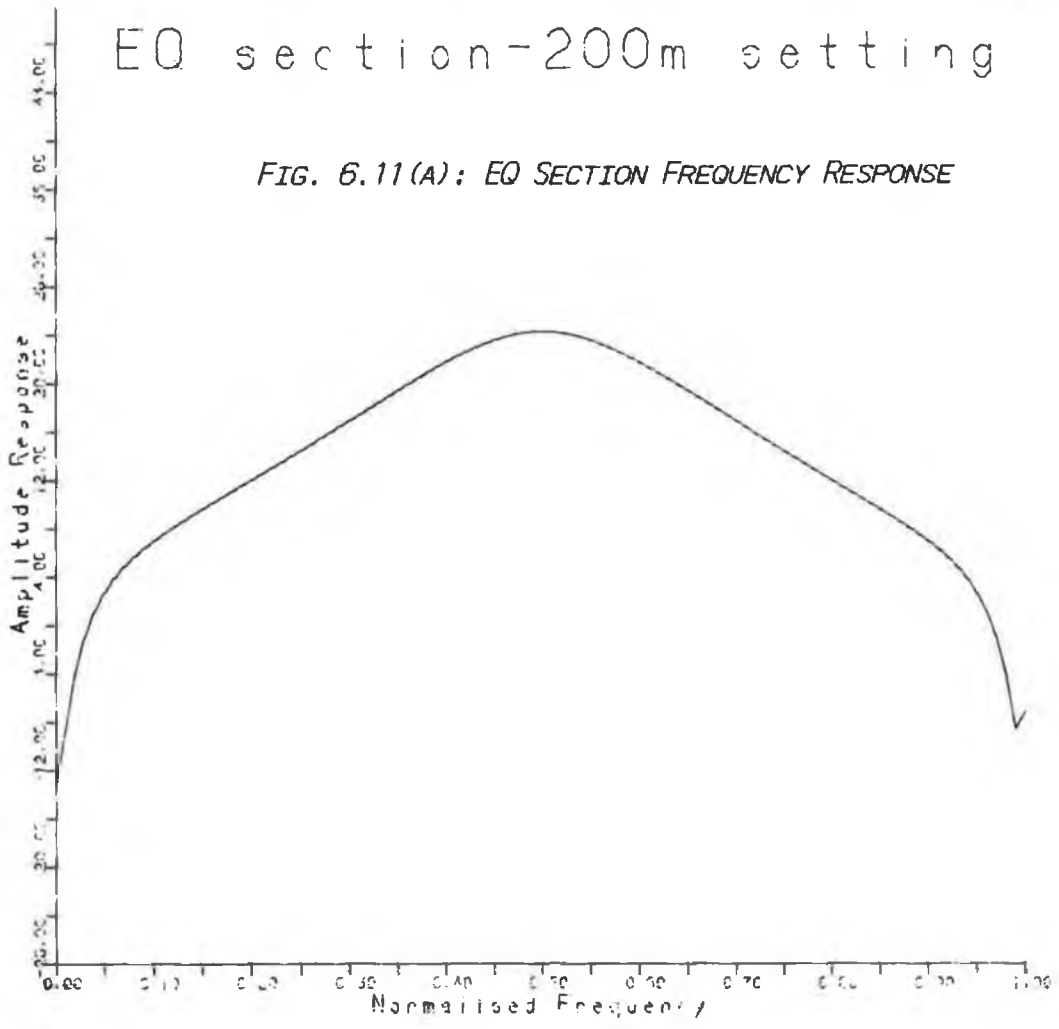


FIG. 6.11(A): EQ SECTION FREQUENCY RESPONSE

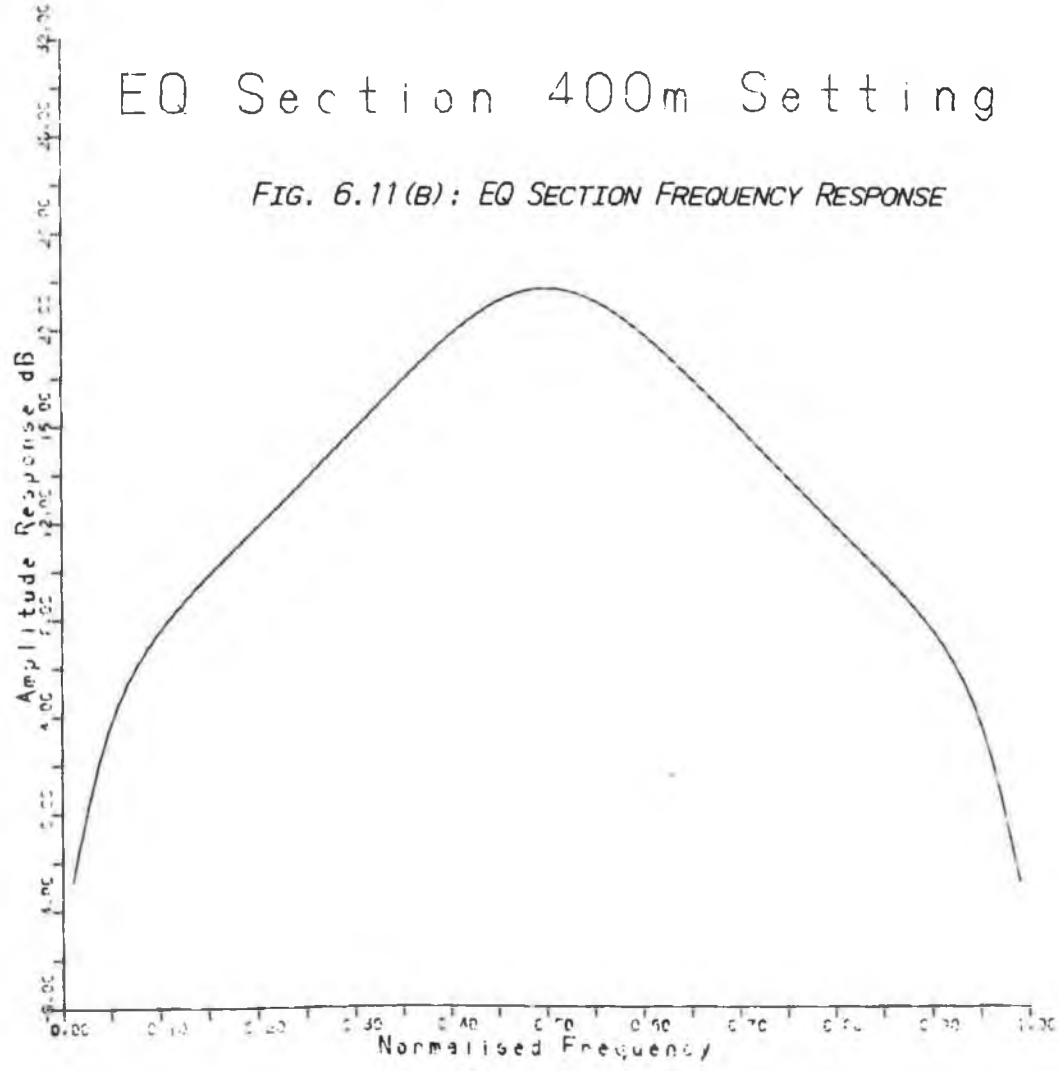


FIG. 6.11(B): EQ SECTION FREQUENCY RESPONSE

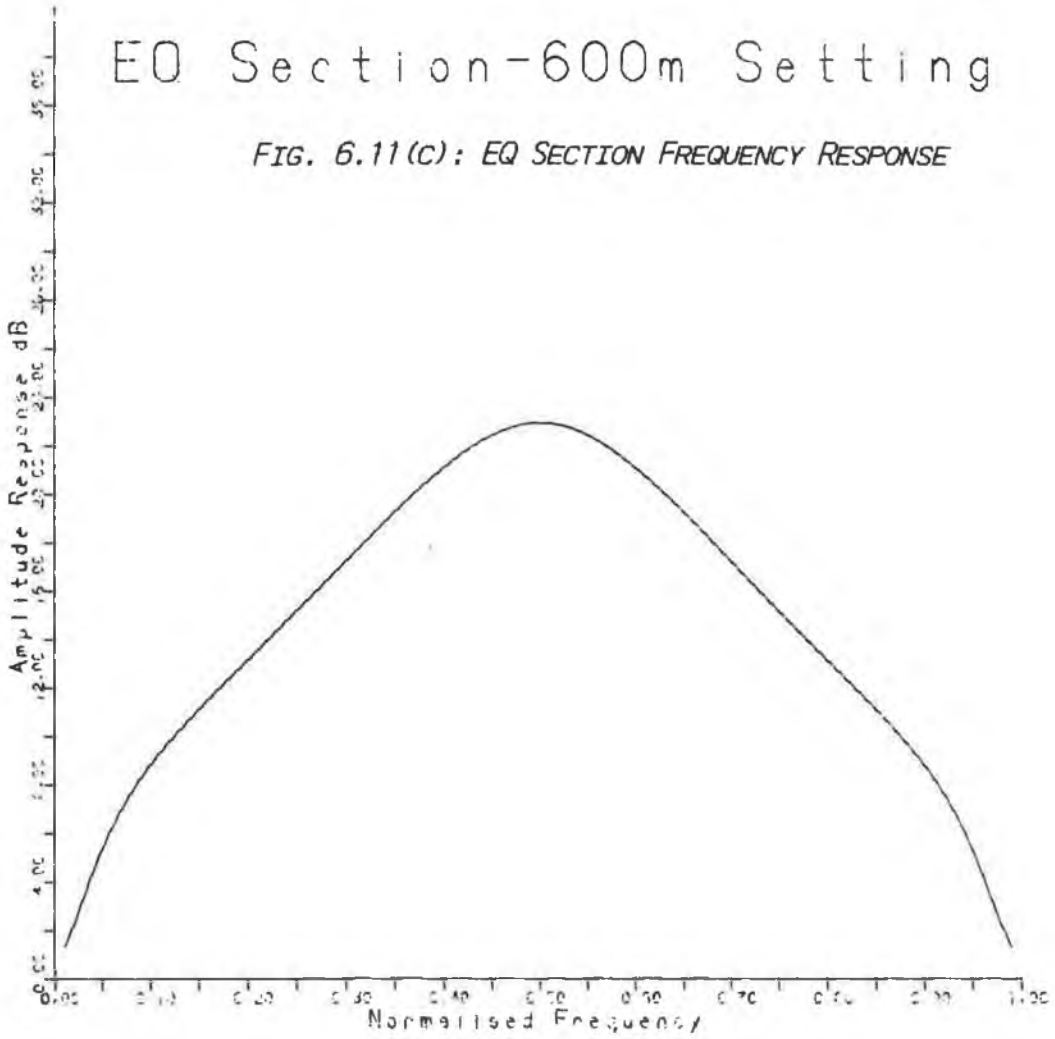


FIG. 6.11(C): EQ SECTION FREQUENCY RESPONSE

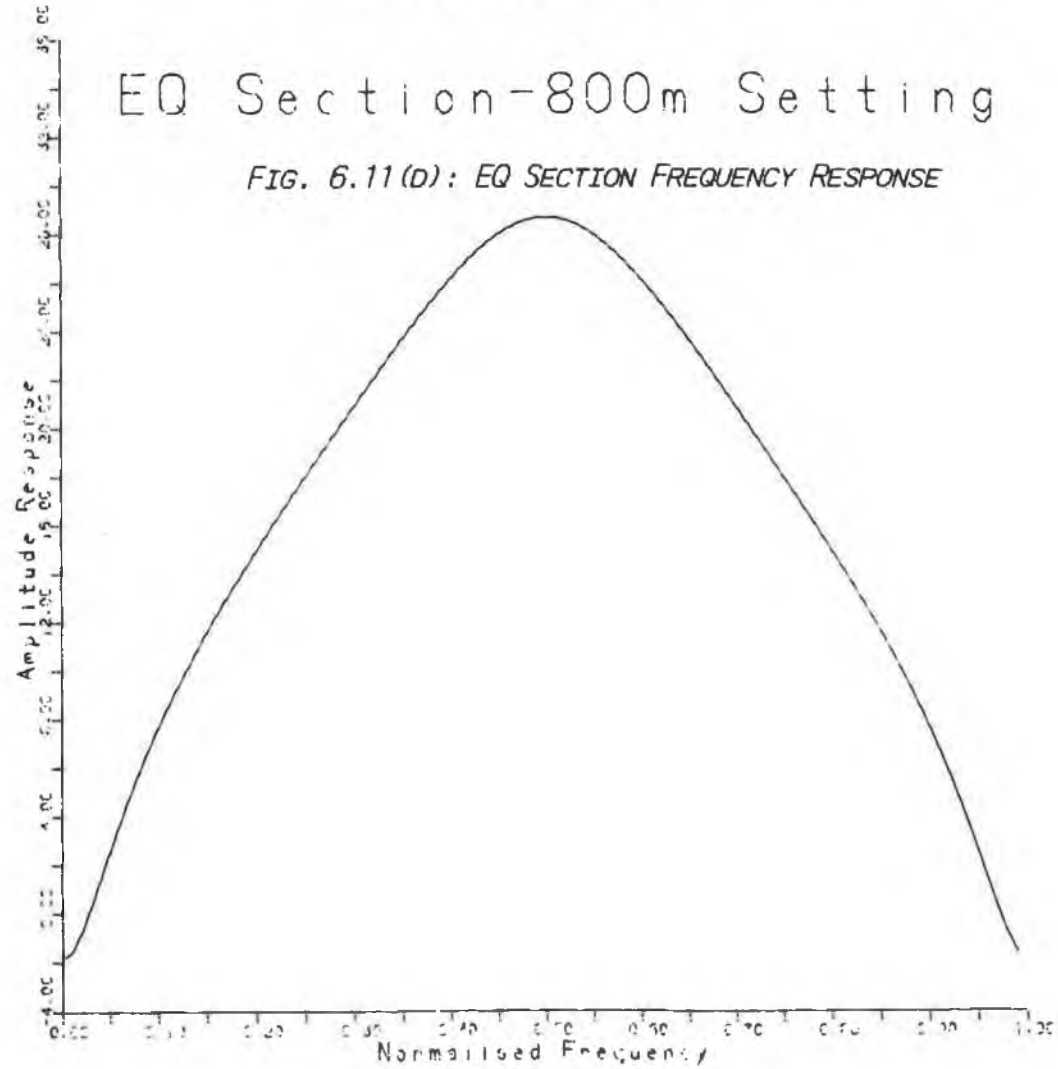


FIG. 6.11(D): EQ SECTION FREQUENCY RESPONSE

Fig. 6.11 indicates that, although the equaliser is successful in reducing inter-symbol interference, this has not been achieved in a finite bandwidth. Thus the equaliser section output contains noise terms which must be filtered out if they are not to degrade the equaliser performance. In [153] a fourth order switched-capacitor filter is used for this purpose. No details are given, but it is presumed that two biquads of the type in [23] are used. The fourth order filter is used to approximate a frequency response given by the 100% raised cosine response of (6.26) and (6.27). Following the equaliser section by such a filter does not result in a significant deterioration of the ISI value, because its impulse response is ideally zero at every second sampling instant away from the response peak, and is low elsewhere. Alternatively, the optimisation can be modified to take account of the presence of the roll-off filter by regarding it as being incorporated in the SC LPF. In this case, the input to the equaliser section in the optimisation software is equivalent to the overall equaliser system output with the equaliser section (excepting the cosine filter at its input) bypassed.

In this way, the poles and zeros can be fine-tuned to take into account the effect of the roll-off filter. A fourth order filter allows a close approximation to (6.26) with a phase response that approximates to linearity. However, this is achieved at the expense of a considerable increase in circuit complexity. A minimal approach to implementing the roll-off filter is to use a damped discrete integrator for the purpose, such as shown in Fig. 6.12. The transfer function of the damped discrete integrator is chosen to give unity gain at d.c. and a gain of 0.5 at a frequency of 0.5 f_B, thereby matching the desired amplitude response at these two points in frequency. Thus the transfer function is

$$F(z) = (1-k)/(1 - k\ z^{-1}) \tag{6.29}$$

with k chosen such that $|F(z)| = 0.5$ when $z = \exp(j\ 2\pi\ f_B/f_S) = (1 - j)/\sqrt{2}$. Thus k = 0.645. This corresponds to the capacitor values :

$C_1 = 1.00$
$C_2 = 3.63$
$C_3 = 2.00$

in Fig. 6.12. The resulting inter-symbol interference, listed in Table 6.5, is still quite acceptable for the four equaliser settings. Unfortunately, the high

frequency attenuation of the equaliser section is still insufficient to meet the chosen specification for alias rejection. Increasing the value of k in (6.29) to 0.95 results in the second set of ISI values shown in Table 6.5. The resulting equaliser section response for the 600m setting is shown in Fig. 6.13. It can be seen that the addition of the damped discrete integrator is sufficient to reduce the gain of the equaliser section in the frequency range from 0.25 f_S to 0.5f_S. However, the average attenuation in this frequency range is about 5 dB, 8 dB short of that required to achieve the specified level for alias rejection, in conjunction with the anti-aliasing stages, which have the response shown in Fig. 6.5.

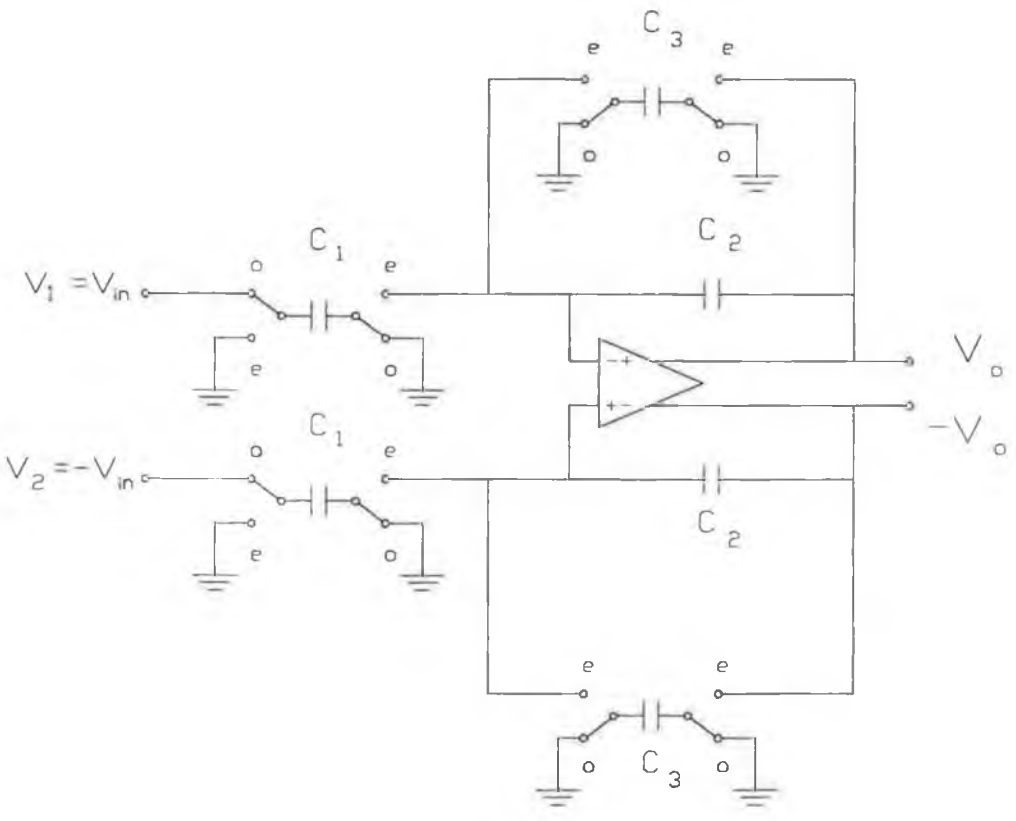


Fig. 6.12: A first-order roll-off filter.

ISI values

line length	k = 0.645	k = 0.950
200m	12.5×10^{-2}	9.42×10^{-2}
400m	11.2×10^{-2}	6.71×10^{-2}
600m	7.24×10^{-2}	4.40×10^{-2}
800m	9.76×10^{-2}	3.09×10^{-2}

Table 6.5: ISI values after low-pass filtering

The inter-symbol interference can be reduced for the above technique by taking account of the effect of the damped discrete integrator on the pulse waveform at the optimisation stage. However, since the line attenuation increases as frequency increases, the optimisation in general then tends to increase the gain of the equaliser section at high frequencies so as to compensate for the roll-off of the damped discrete integrator. This obviously counters the usefulness of the integrator as a roll-off filter.

A solution to the above problem is to modify the objective function used for time domain optimisation so as to include a frequency domain measurement as well as the time domain measurement of the inter-symbol interference. Specifically, the optimisation could be modified so as to minimise the inter-symbol interference of the system whilst also minimising the equaliser section gain for frequencies beyond f_B. A similar hybrid criterion is used in [181] for the design of digital FIR Nyquist filters.

6.5.2: Frequency Domain Results.

In order to compare the frequency domain technique to that already considered for the time domain, it has been applied to the case of an 800m line length. The amplitude (both on a linear scale, and in dB) of the transfer function

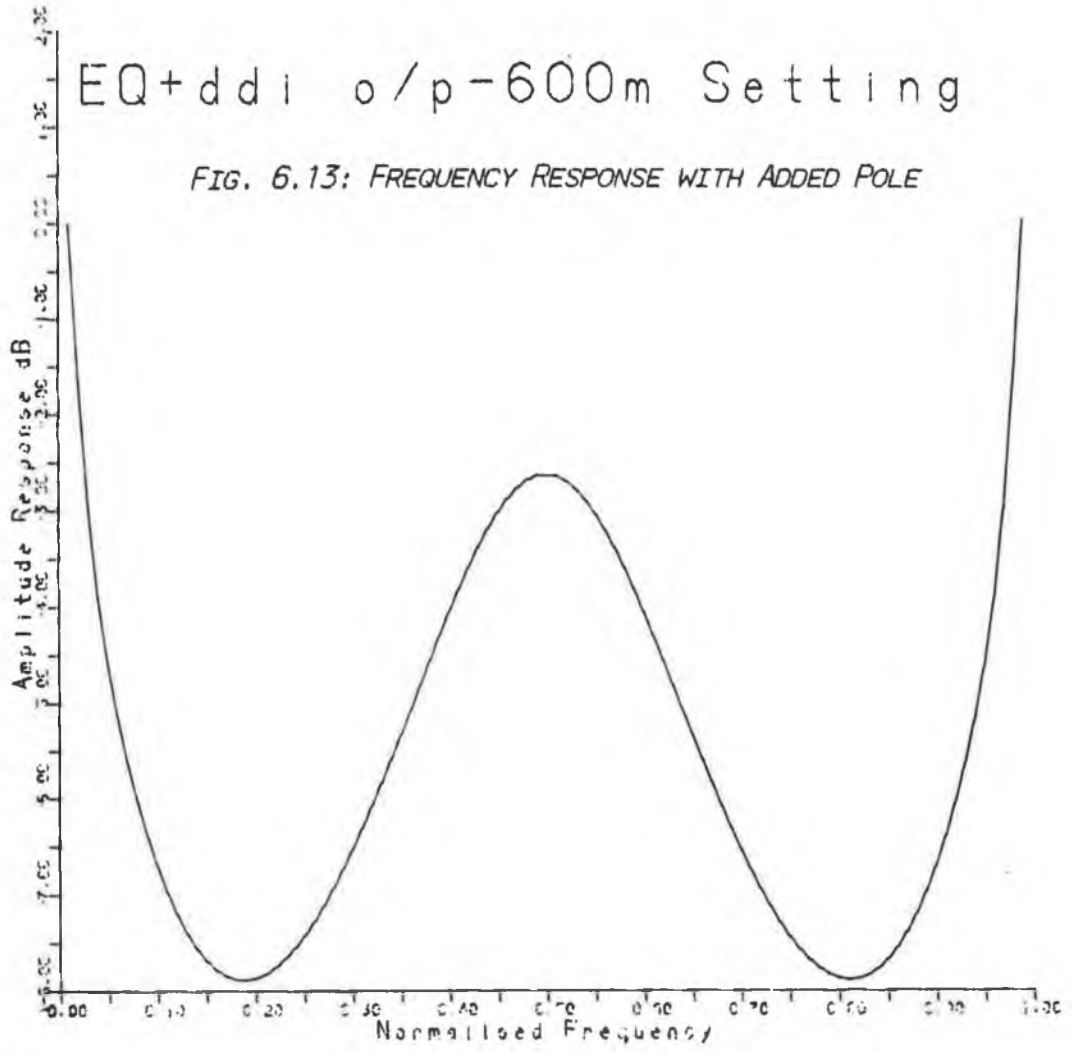


FIG. 6.13: FREQUENCY RESPONSE WITH ADDED POLE

of a line of this length, as calculated by the simulation program, is shown in Fig. 6.14.

The results obtained using this method depend on the weights used in calculating the objective function to be minimised, as a linear function of the phase error and magnitude error in the equaliser output. It has not been possible to reduce both phase and magnitude errors to low values simultaneously. Two sets of results are presented, based on different weightings. These are shown in Table 6.6.

	Set 1	Set 2
K	1.91	0.34
b_0	0.51	0.54
b_1	0.52	0.41
b_2	-0.89	0.24
a_0	-2.01	-6.14
a_1	0.76	0.77
ISI	12.7×10^{-2}	11.9×10^{-2}
C_{1a_1}	-4.02	5.08
C_{1b_1}	1.00	-1.00
C_{21}	2.17	4.00
C_{31}	-3.78	9.56
C_{12}	1.50	1.00
C_{22}	2.00	4.56
C_{32}	4.00	9.12
C_{1a_3}	1.90	1.00
C_{1b_3}	2.39	9.65
C_{1c_3}	-1.75	-19.3
C_{23}	1.02	3.25
C_{33}	1.00	2.78

Table 6.6 : Results for the frequency domain optimisation

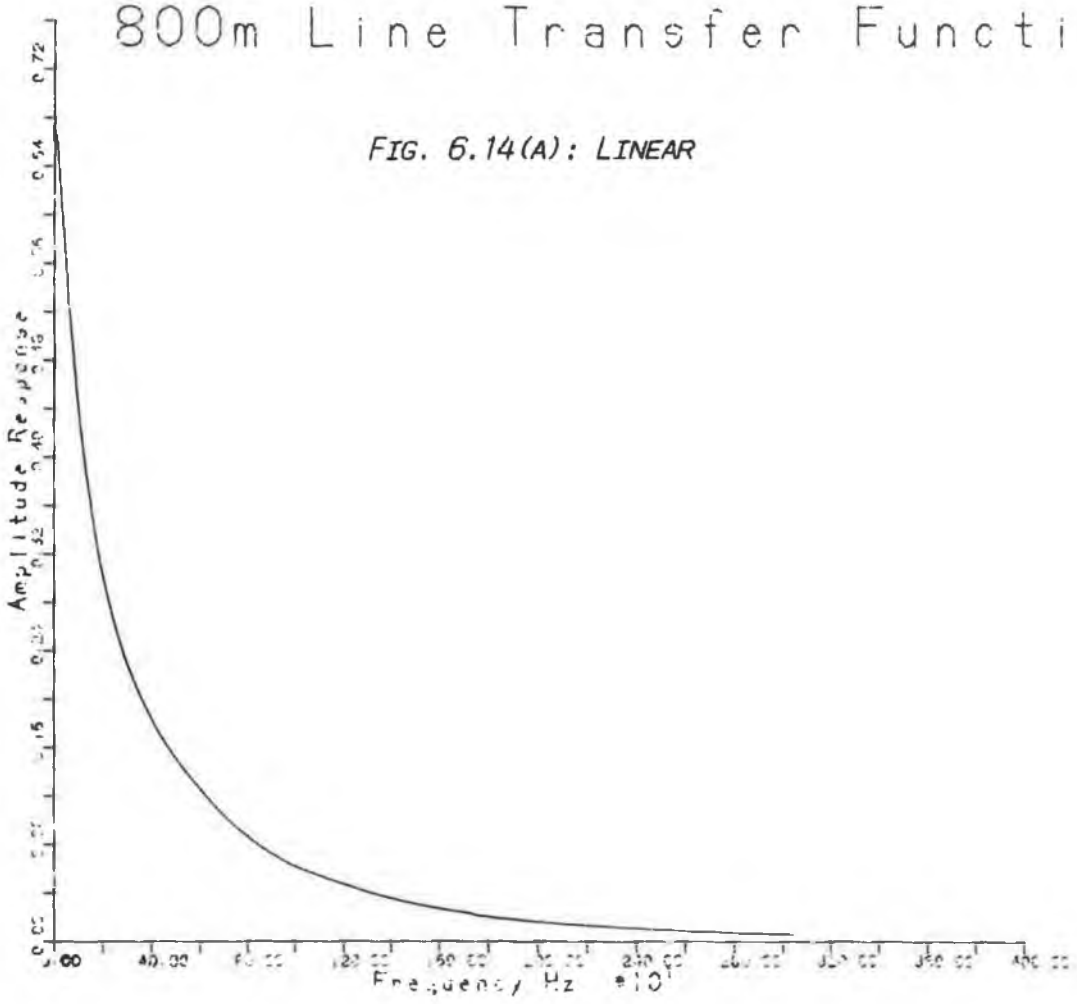


FIG. 6.14(A): LINEAR

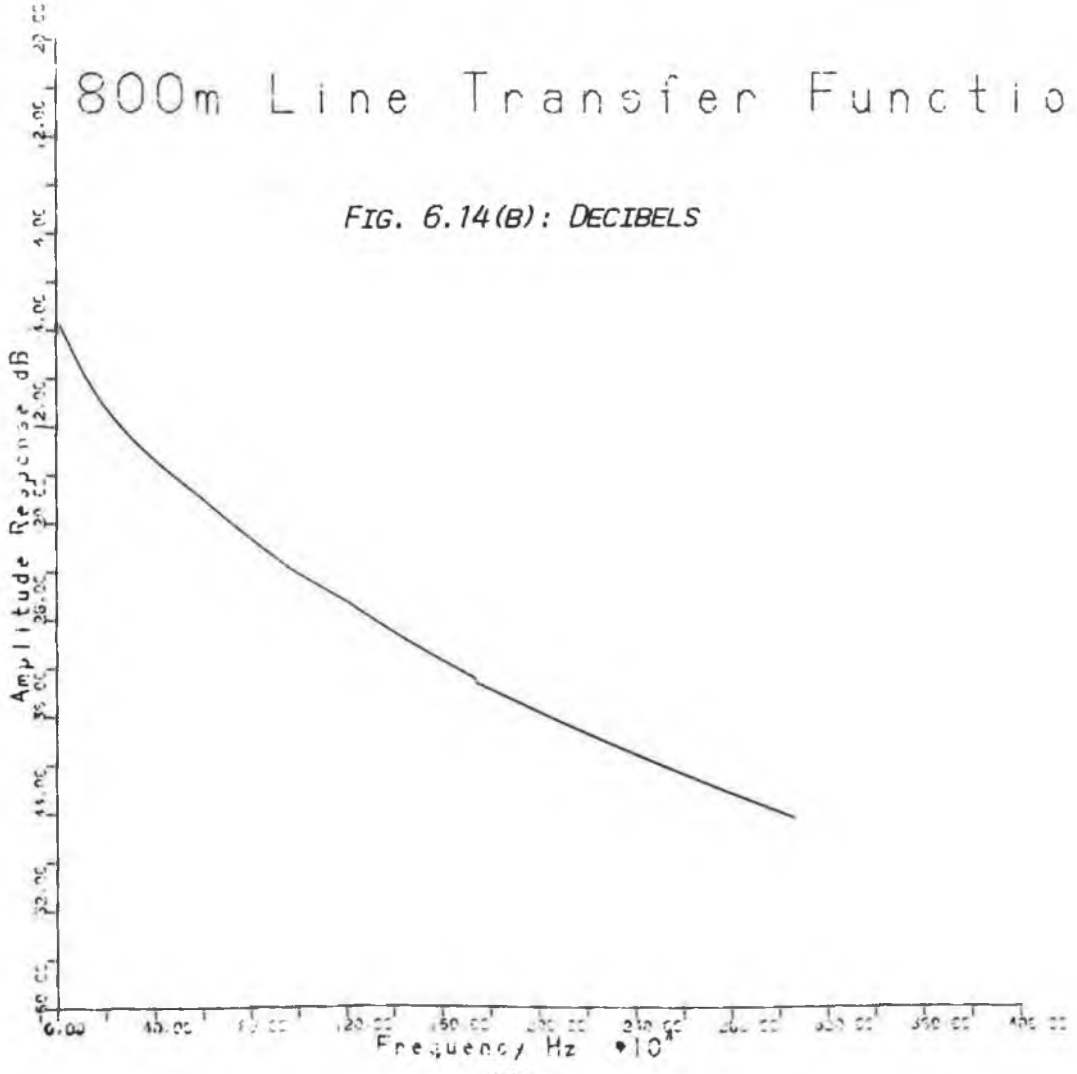


FIG. 6.14(B): DECIBELS

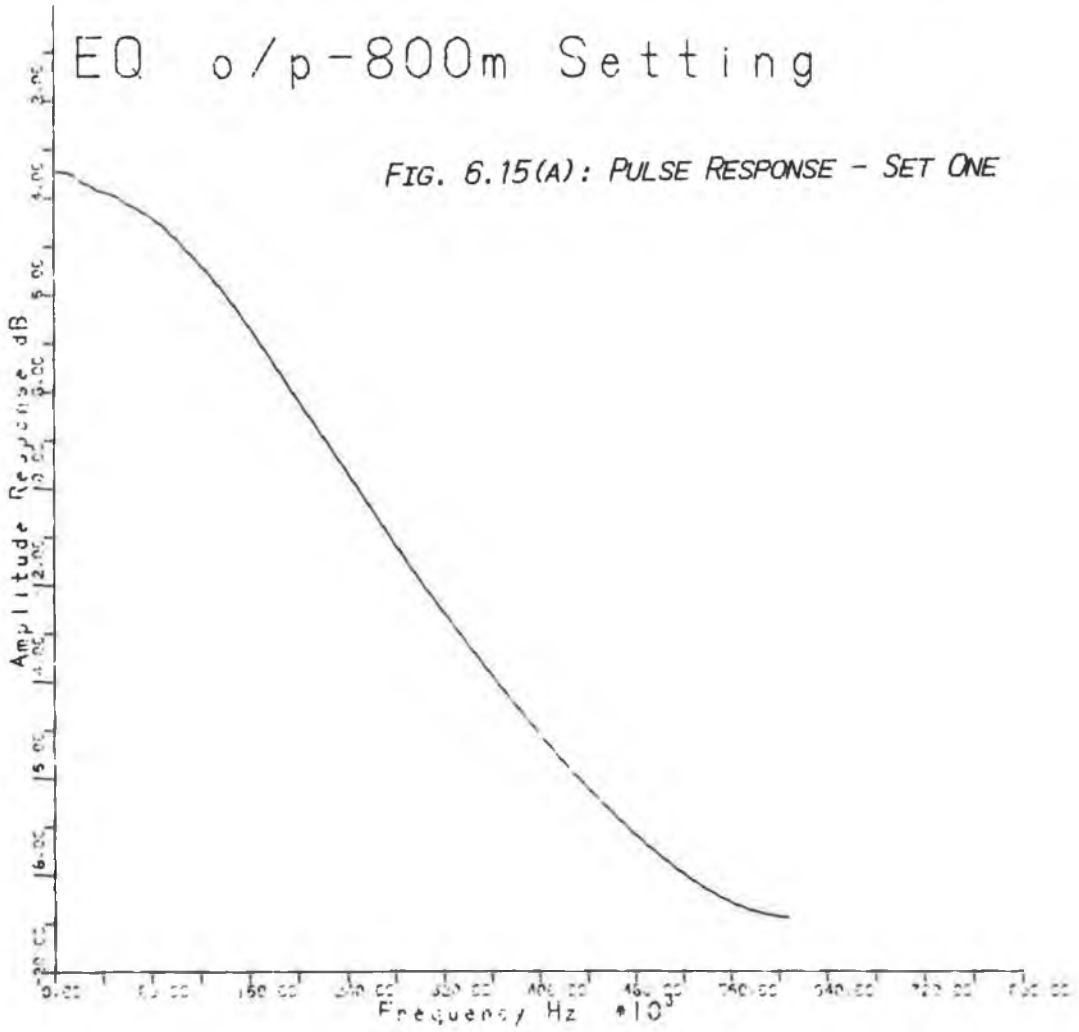


FIG. 6.15(A): PULSE RESPONSE - SET ONE

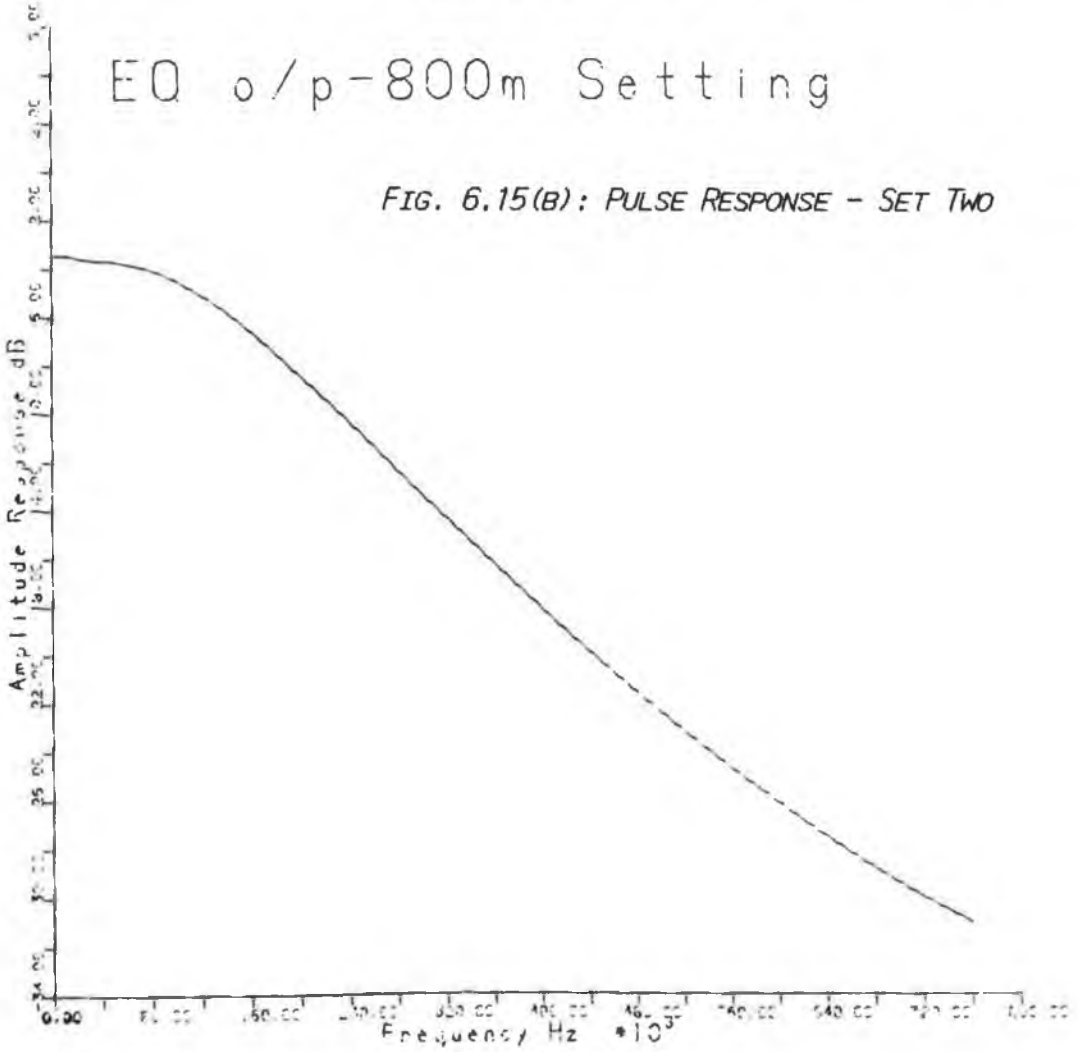


FIG. 6.15(B): PULSE RESPONSE - SET TWO

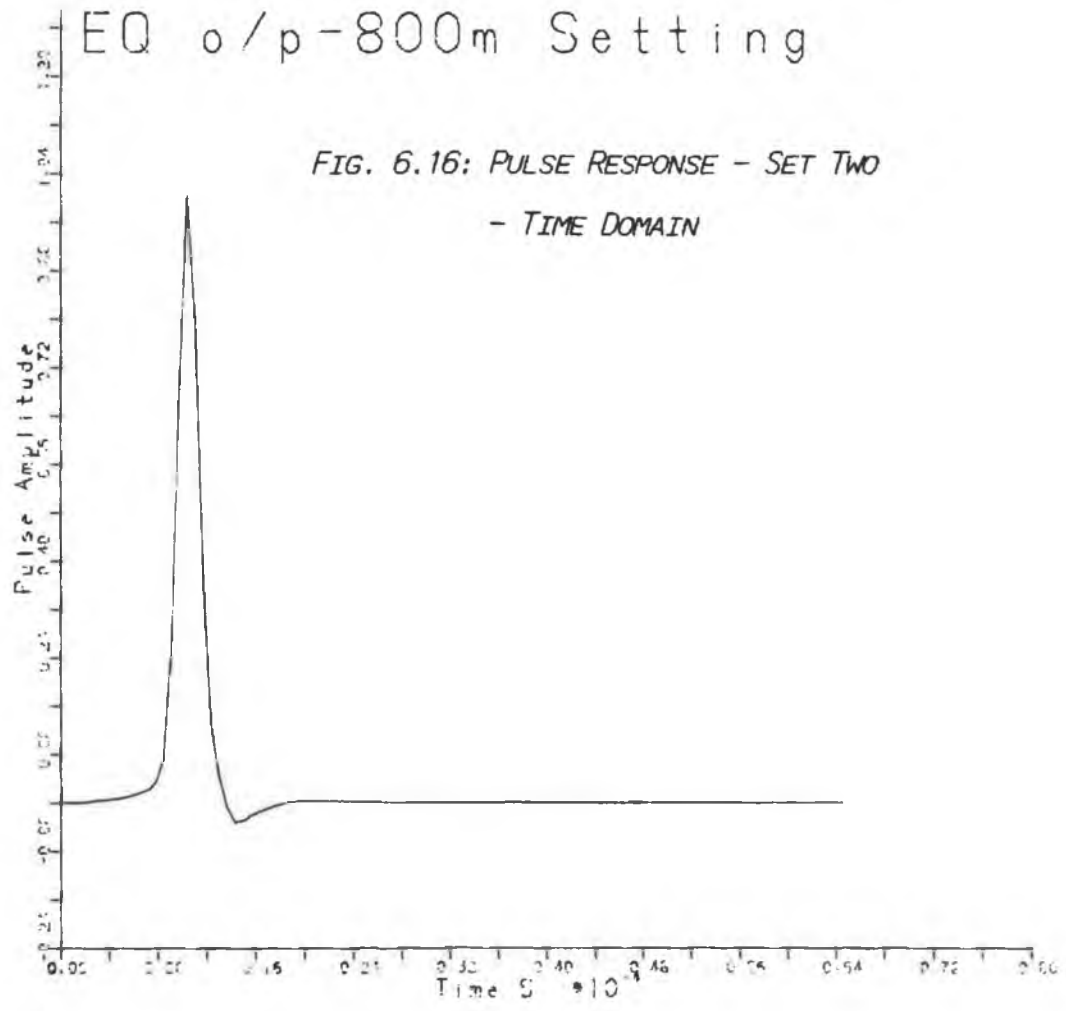


FIG. 6.16: PULSE RESPONSE - SET TWO - TIME DOMAIN

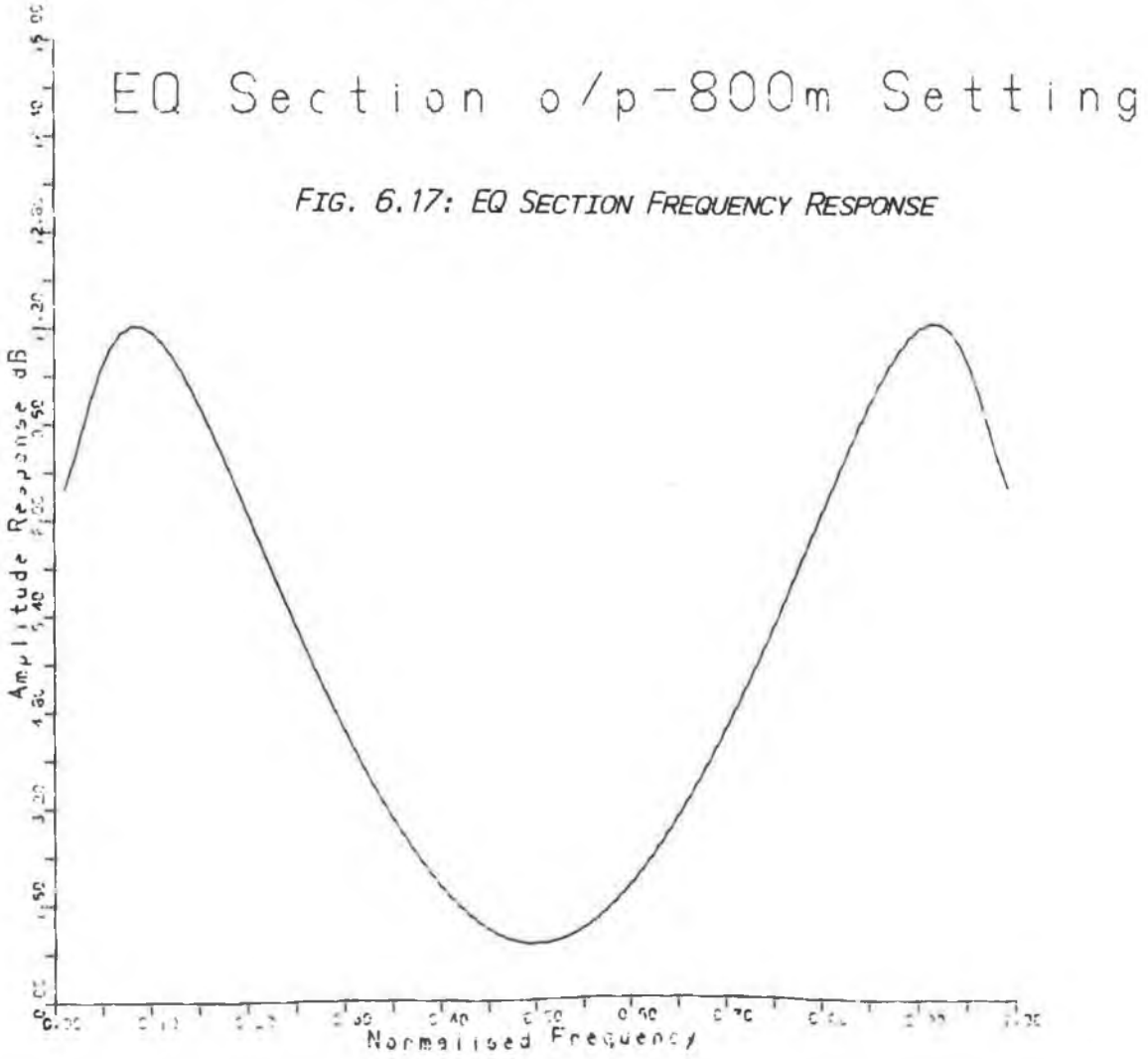


FIG. 6.17: EQ SECTION FREQUENCY RESPONSE

The pole locations in the above table differ substantially from those in Table 6.3, due to the necessity of introducing high frequency attenuation using the frequency domain technique. As a consequence, the results obtained for ISI are inferior, and the capacitance spread is higher than that obtained using the time domain method, even though every capacitor value has been allowed to vary, so as to minimise the spread. Thus a price has been paid for the frequency selectivity of the resulting equaliser section.

The equaliser output for a pulse applied at the line input is shown in Fig. 6.15(a) and Fig. 6.15(b) for the first and second sets of results in Table 6.6 respectively. It can be seen that the responses are only approximately in the form of a raised- cosine pulse. However, they do result in low values for ISI. For example, the time domain pulse response corresponding to Fig. 6.15(b) is shown in Fig. 6.16. Also the equaliser section response rolls off up to the Nyquist frequency, as shown by the amplitude response plot of Fig. 6.17 , for the second set of poles and zeros in Table 6.6.

6.5.3: Conclusions

The experience obtained in applying the time domain and frequency domain optimisation techniques suggests that a hybrid technique, as earlier suggested, may be the easiest to apply. This avoids the chief difficulty of the time domain method (the absence of control over the frequency response) and also of the frequency domain method (weightings must be assigned to the phase and amplitude errors). The use of an equaliser section with an additional z-plane pole in the transfer function should make it easier to satisfy the conflicting requirements of finite equaliser section bandwidth, low capacitance ratio spread, and low ISI.

6.6: Adaptation of the Equaliser.

6.6.1: Previous Algorithms.

As discussed in Chapter Two, a number of line equaliser techniques have been developed, based upon switched- capacitor filtering techniques, which feature adaptive operation.

The majority of these equalisers operate simply by using automatic gain control to regulate the level of the equaliser output. The gain setting required is obviously proportional to the attenuation introduced by the line, which increases as the line length increases. Thus the required gain setting indicates approximately the length of the line. By incorporating a change in the equaliser transfer function appropriate to that line length with that gain setting, the automatic gain control also causes the equaliser response to adapt for minimum inter-symbol interference.

The descriptions of the algorithms used given in the literature have been lacking in specifics. In [145] the adaptation is said to be done as follows :

Adaptation is performed by adjusting the settings for gain and equalisation so that the average level of output matches a desired reference value. The settings are controlled by the "accumulated sgn(e_k)" (which equals unity if the output exceeds the reference level, and equals minus one if the output is below the required level). This accumulated signal "organizes 9 bits of digital data" (in an unspecified manner). Six of the bits control the gain, and three control the equalisation. This 'orgainisation' is presumably implemented using counters.

The counters can be regarded as introducing inertia or damping into the control algorithm, preventing the equaliser from 'hunting' from one setting to another in a spurious fashion. A possible way to achieve this is as follows :

The gain control is split into a fine gain control and a coarse gain control. The counter is similarly divided into two 2's complement counters, which shall be referred to as the upper counter and the lower counter. Both counters are initially reset to zero. The lower counter is incremented or decremented every time a mark is received (that is, when the magnitude of the equaliser output exceeds half the reference level for a mark - $|V_{EQ}| > \frac{1}{2} V_{REF}$). If the equaliser output is too high ($|V_{EQ}| > V_{REF}$) the count is incremented, otherwise it is decremented. Consequently, if the equaliser is correctly set, there are on average an equal number of received pulses above and below the reference level and the count will remain close to zero. If, however, the equaliser gain is incorrectly set, then the count will either persistently increment or persistently decrement. Thus, an overflow or underflow of the lower counter is indicative of the equaliser gain

being too high or too low respectively.

When this occurs, it precipitates the following actions. The lower counter is reset to zero, the fine gain is increased to its next increment (for an underflow) or decreased (for an overflow) and the upper counter is incremented (decremented) for an overflow (underflow). The coarse gain is similarly controlled by the upper counter, which will overflow or underflow if the equaliser gain is far from the correct level. The use of counters in this way ensures that the gain control does not respond instantaneously to changes in the received level of pulses, but rather responds to trends in the received level. Obviously the counter lengths must be determined as a compromise between the time taken to converge to the correct gain, and immunity to transients caused by noise or by changes in the equaliser settings.

A second algorithm for automatic gain control is that used in [153] to control an equaliser of the type in Fig. 2.5. This can be described by the flowchart of Fig. 6.18.

In this algorithm, the 'time constant' or damping is provided more simply, by simply requiring that a gain error persist for the duration of half a burst before it is acted upon.

The above algorithms are limited by their lack of flexibility. They assume a frequency response for the line based on a single measurement i.e. the height of the output pulse from the line. This limits their application to lines of a particular type - for example, the equaliser in [145] is designed for 0.4 mm diameter lines with polyethylene insulation.

An algorithm which, at least in principle, is more capable of operating with various line types is that described in [155]. The approach here is to separate the automatic gain control function and the frequency response adaptation. The automatic gain control performs similarly to the techniques described earlier. When the gain of the equaliser is correctly set, the equaliser output at a high frequency is estimated by applying it to a band pass filter, and measuring the resulting

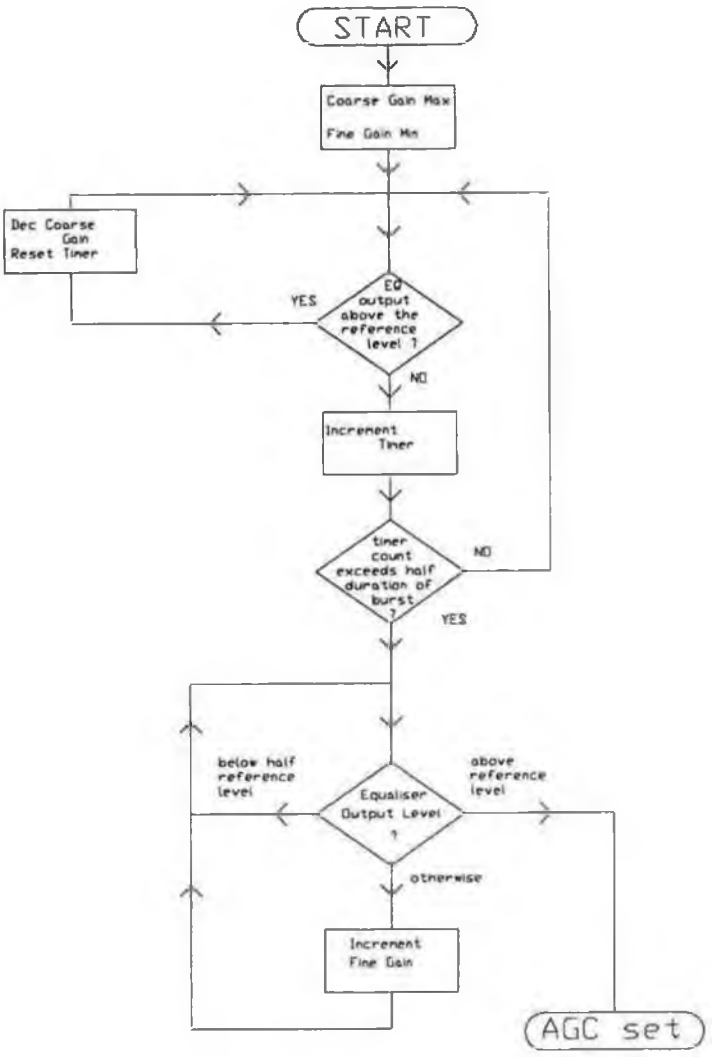


Fig. 6.18: Adaptation of NTT equaliser

output. From this level, the slope of the frequency rolloff of the channel is estimated, and the equaliser transfer dunction is switched to the most suitable response. This is similar to the technique used in [154] where a filter referred to as a slope equaliser is used to compensate for the high frequency response of the channel.

6.6.2: Proposed Algorithm.

The details of an algorithm based on the principle described in [155] will now be given. The structure of the bandpass filter to be used is shown in Fig. 6.19. A flowchart of the proposed algorithm is shown in Fig. 6.20. A brief description of the algorithm will now be given. CGC is the coarse gain setting, variable from 0 (minimum gain) to 7 (maximum gain). FGC is the fine gain adjustment, adjustable from 0 to 15. EQ is the setting of the equaliser section. There are n such settings, the number n depending on the range of line lengths to which the equaliser is to be capable of adapting, and the maximum value of inter-symbol interference tolerated. In the situation where it is desired to integrate the equaliser system on one chip, the value of n will also be technology dependent, since increasing n increases the die area occupied by programmable capacitor arrays significantly, the amount of increase depending on the size of unit capacitor used in the particular technology. The EQ setting can be varied from 0 (for short lines) to n-1 (for longer lines).

The value of CGC is initially set to its maximum. This ensures that, if a signal is present on the line, it will produce a saturated output at the equaliser output V_{EQ}. If the output is at a low level, no signal is assumed to be present (only noise) and so the adaptation algorithm is suspended. This is done by comparing the level of V_{EQ} to a value, V_{TRSHLD}, chosen to be midway between the optimal value of V_{OUT} (i.e. V_{REF}) and the value obtained due to noise, with the input earthed. If the level of V_{EQ} is too low, adaptation does not proceed. Otherwise, V_{EQ} is checked to see if it is in a window of acceptable levels, i.e. to see if

$$V_{REFMIN} < |V_{EQ}| < V_{REFMAX}$$

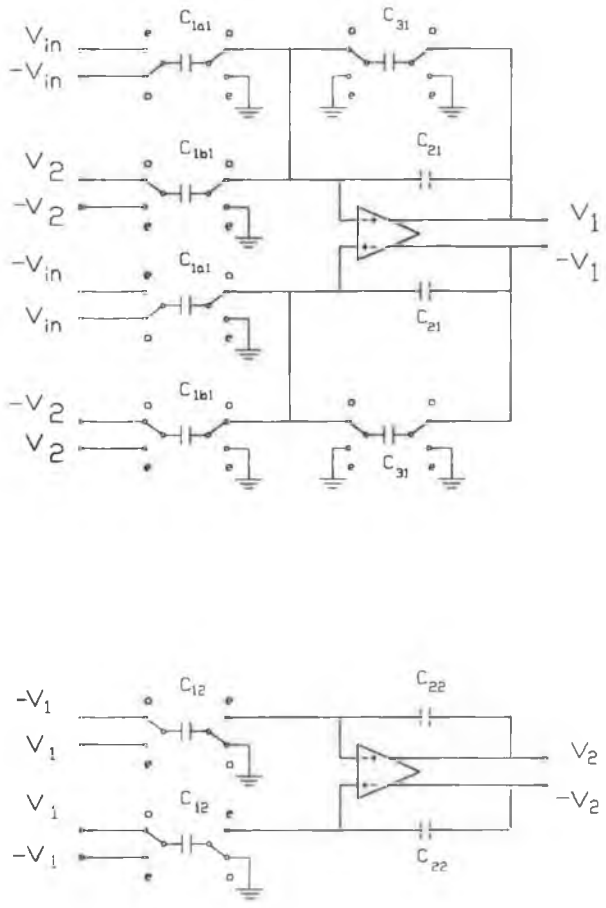


Fig. 6.19: Slope Estimation Filter

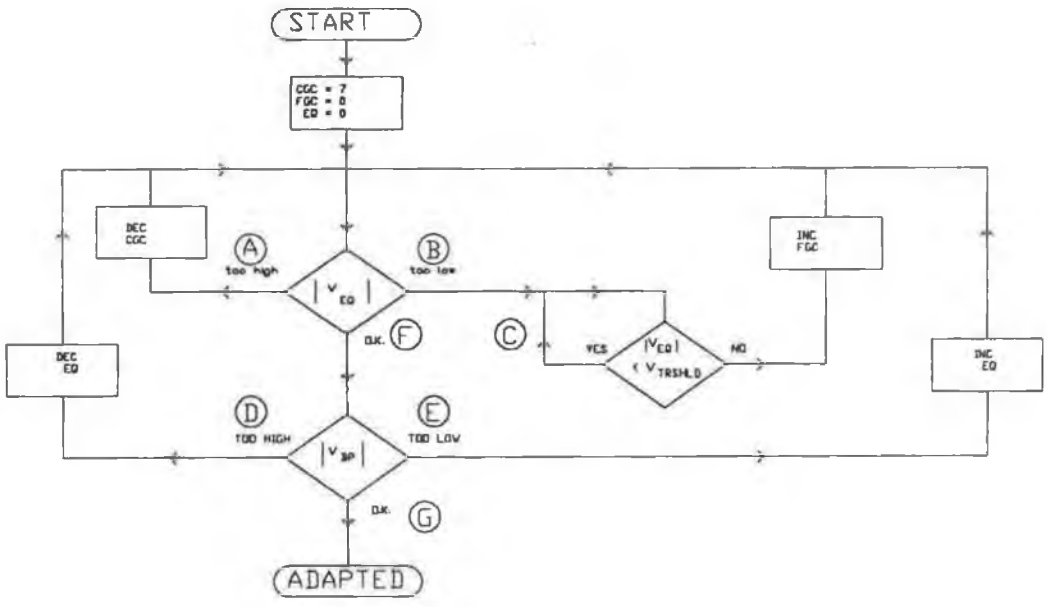
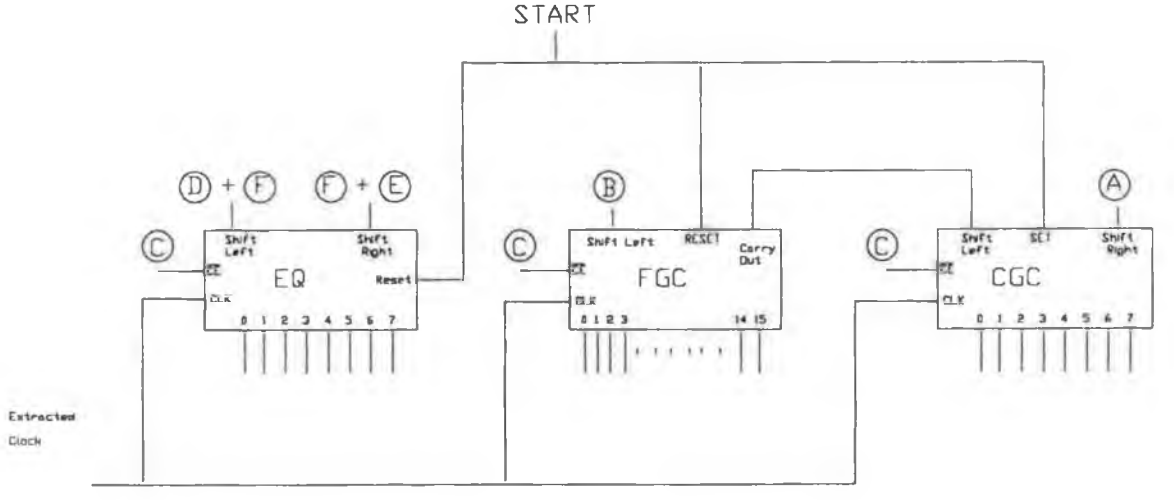


Fig. 6.20: Proposed Adaptation Algorithm.



Notes: 1) EQ, FGC, and CGC are shift registers.
2) Input C disables the other register inputs.
3) Inputs A,B,..,F are obtained using comparators.

Fig. 6.21: Circuitry to implement proposed algorithm.

where V_{REFMIN}, V_{REFMAX} are chosen to be equal to V_{REF} ± an acceptable tolerance. If the output level is too high, it is reduced by lowering the coarse gain setting CGC. If it is too low, it is increased by increasing the fine gain setting FGC. If V_{EQ} is within the acceptable limits, then the gain control is at the correct setting.

To check for the correct EQ setting, the equaliser output is applied to the band pass filter, whose output V_{BP} is compared to a window of acceptable levels i.e. the control algorithm checks if

$$V_{BPMIN} < |V_{BP}| < V_{BPMAX}$$

If the equaliser is correctly set, then the system (pulse + channel + equaliser) frequency response should be flat up to half the bit rate , and should roll off thereafter (assuming a frequency domain optimisation based on the 100% raised cosine response). However, if the equaliser is incorrectly set, then the response up to $\frac{1}{2}f_B$ will not be flat. Instead it will rise with frequency up to $\frac{1}{2}f_B$ (over-equalisation - the equaliser is adjusted for a line which is longer than that actually present) or will fall with frequency up to $\frac{1}{2}f_B$ (under-equalisation). Thus in the case of under-equalisation (overequalisation) ,the band pass filter output will be at too low (high) a level, and the next higher (lower) equaliser setting must be selected. In this way, the equaliser section will adapt to its correct setting.

In the algorithm of Fig. 6.20 no provision has been made for a 'time constant'. This feature can readily be incorporated using counters to ensure that the outputs of the equaliser section and the bandpass filter must be outside their windows of correct values for a duration corresponding to a number of bit intervals, before the equaliser control algorithm is affected by them. Fig. 6.21 shows a possible circuit for the implementation of the algorithm of Fig. 6.20.

6.7: Filter Sections Fabricated.

The motivation for using switched- capacitor techniques when designing a filter is that the resulting circuit can be integrated on a MOS process. Thus the goal in designing the circuits in this chapter has been to produce filter sections which are suitable for integration on the CMOS process available at the National Micro-electronics Research Centre (N.M.R.C.) in Cork. Thus this work has been carried out in conjunction with the N.M.R.C.

The CMOS process used at the N.M.R.C. features a 5 μm feature size, self-aligned polysilicon gate and a p-type substrate. Prior to the present work, it had not been used for the fabrication of switched- capacitor circuits. Two new processing steps have been introduced to facilitate the integration of switched-capacitor filters, specifically the addition of a second polysilicon layer, thereby allowing 'poly-poly' capacitors to be fabricated, and an n^+ implant, also used for fabricating capacitors.

The results of the equaliser design have been made available to the N.M.R.C., to allow test circuits to be integrated, thus allowing the equaliser system to be evaluated. To allow the capabilities of switched- capacitor filters fabricated using the N.M.R.C.'s CMOS process to be determined, the following mask sets have been integrated at the N.M.R.C.:

1) A mask set containing arrays of capacitors and several op-amps. This has been implemented using a single layer of polysilicon, and has allowed measurements to be made of the properties of the various capacitor types, in particular the variation in capacitance with applied voltage, and the precision of the capacitor ratios attainable. For example, it has been found that an accuracy within 0.26 % can be maintained, for a capacitance ratio spread of 16:1, if all the capacitor values are integer multiples of a unit capacitor value of 0.8 pF.

2) A mask set featuring a number of low-pass filter circuits. The capacitor ratios for these filters, which are stray-sensitive switched- capacitor ladder filters of the type shown in Fig. 3.1, have been obtained using the synthesis program developed in Chapter Three. Third, fourth, and fifth order filters have been integrated, featuring both maximally-flat and equiripple passband responses. Also, a

first order filter stage, featuring a programmable capacitor array of the type in [136] has been incorporated in the mask set.

The sequence in which these mask sets have been prepared reflects the historical development of switched- capacitor filters, described briefly in Chapter Two. Thus, precision ratioed capacitors and integrable MOS op-amps are a pre-requisite for the fabrication of switched- capacitor filters, and these have been tested on the first mask set. The earliest designs for switched- capacitor filters were stray-sensitive, and filters of this type have been integrated on the second mask set.

The experience gained at the N.M.R.C. with the above mask sets has been applied to the integration of a number of the circuits presented in this chapter. These are:

1) The continuous-time section of Fig. 6.2(a). Where resistor and capacitor values have been scaled in Section 6.3, this has been done in accordance with recommendations from the N.M.R.C. so as to produce values suitable for integration. In order to simplify the amount of digital circuitry required, every second switch in the tapped resistor chains for the coarse-gain and fine-gain adjustment has been left out of the circuit to be fabricated, so that the range of gain variation possible is reduced. However, the available level of programmability is sufficient to test the gain control technique used.

2) The switched-capacitor low-pass filter of Fig. 6.2(b). This has been implemented as designed earlier.

3) The equaliser section of Fig. 6.3. This has been designed to implement the transfer functions listed in Table 6.7, which represent a provisional set of results obtained using the time-domain optimisation technique of Section 6.6 at the time when element values for the circuits in the third mask set were being finalised. Because the zeros occur at different regions of the z-plane for the 200m and 600m settings, as compared with the 400m and 800m settings, two different circuit topologies are required, using the circuit transformations described in Chapter Five. The programmability must thus extend to the control of the polarity of the inputs

from the first and second stages of the equaliser section to capacitors C_{1b3} and C_{1c3} respectively. This is achieved using MOS switches with appropriate control logic. The capacitance ratio spread for the equaliser section, when designed to implement the set of transfer functions in Table 6.7 is 15.3:1.

line length	K	b_0	b_1	b_2	a_0	a_1
200m	2.45	0.231	-0.210	-0.790	0.303	-1.72
400m	0.883	0.231	-0.241	-0.200	0.499	7.10
600m	0.718	0.646	-0.818	-0.075	0.809	-8.85
800m	1.52	0.601	-0.182	-0.360	3.21	0.829

Table 6.7: Transfer Functions for Fabricated Equaliser Section

4) The bandpass filter of Fig. 6.19. This has been designed to the same specification as that for the corresponding filter in [155], i.e. it has a centre frequency of 240 kHz and a Q of 2.45, and features a unity passband gain. It can readily shown that, for a sampling rate of 1.536 MHz, the filter should have the transfer function

$$H(z) = \frac{1 - z^{-2}}{7.01 - 6.68\, z^{-1} + 5.01\, z^{-2}} \qquad (6.30)$$

The resulting filter has a capacitance ratio spread of 10.02:1. The circuit in Fig. 6.19 is identical to the bandpass filter investigated in [59], which has a transfer function numerator of the form $1-z^{-1}$, but with the use of a differencing-input for V_{in}, which introduces a factor $1+z^{-1}$ in the numerator of the transfer function, when the equaliser section output in Fig. 6.3 is applied to the bandpass filter input. This follows from the property of differencing-input integrators described by equation (A.46) in Appendix A.

The four test circuits described above allow the potential of the circuitry proposed in this chapter for a switched- capacitor line equaliser to be evaluated. At the time of writing, no results are available for the performance of

these filters, because of the time interval between completion of a mask set and fabrication of the circuit on the N.M.R.C. CMOS process.

Chapter Seven: CONCLUSIONS.

A number of issues relevant to the operation of switched- capacitor filters at high frequencies have been considered, covering both the theory of operation of such filters, and practical considerations of the limitations of integrated designs.

Software has been developed for the exact synthesis of low-pass switched- capacitor ladder filters. Excellent results have been obtained for low-order filters, where there is negligible error between the amplitude response of the synthesised filter in the passband, and the low-pass approximation it is intended to implement, assuming that the capacitor ratios obtained using the synthesis program can be realised precisely. Thus, the program represents a powerful design tool, since filters with equiripple or maximally flat passband responses can be designed in seconds. However, unlike the case for LC lowpass ladder filters, where the maturity of the relevant circuit theory is such that explicit formulae are available for the ladder elements [162], the capacitor ratios for switched- capacitor ladder filters must be obtained using formal synthesis procedures, involving the successive extraction of elements from the input impedance of the ladder circuit. Inevitably, numerical errors accumulate to the point where, for a filter of sufficiently high order, the element values obtained by synthesis are not such as to realise the intended transfer function.

It has been shown that the method of synthesis proposed in [87] has been less sensitive to numerical problems of this kind than its predecessors. Whereas other synthesis techniques fail for filter orders higher than eight, filters of order as high as fifteen can be realised using this technique. It has been found however that, for example, the order of filter which can be synthesised for an equiripple passband response is dependent on the values specified for the cutoff frequency and the passband ripple. Obviously, these limits on the achievable filter order are not absolute, since it is the precision of the arithmetic used in performing the synthesis which determines the amount of error introduced. However, it is felt that they would be typical of the results obtainable using double-precision arithmetic in, for example, most implementations of FORTRAN.

Given the dramatic improvement in the results obtained using the technique of [87], instead of earlier techniques, it is possible that new methods may be discovered which avoid the numerical difficulties which remain in the method of [87], and which thereby allow the order of filter which may be synthesised to be increased. Further investigation into alternative synthesis techniques is thus justified. Another area of interest is the application of the technique of [87] to other filter types, such as bandpass, highpass and linear phase filters [91,96,98], to see if its numerical advantages extend to these filter types.

Software for the evaluation of the sensitivities of the squared-amplitude response of a switched- capacitor ladder filter to variations in its element values has been presented. This allows the hypothesis that switched- capacitor ladder filters feature low passband sensitivity to be verified. The results presented have demonstrated that these filters, when designed for an equiripple passband response, possess low passband sensitivity, but that this sensitivity is non-zero at the peaks in the passband response. This contrasts with the properties of conventional doubly-terminated LC ladders, which can be designed to feature zero sensitivity at the maxima of the passband response. This zero sensitivity occurs because maximum power transfer can be achieved at these points. However, the equivalent circuit of the switched- capacitor ladder filter features terminations whose resistance varies with frequency, and so the peaks in the passband response no longer co-incide with points of maximum power transfer. Thus the sensitivity properties of the LC ladder filter have not been reproduced in the switched- capacitor ladder filter.

To verify this result, switched- capacitor ladder filters which feature a transducer power gain which is equiripple in the passband have been synthesised, and have been shown to feature lower sensitivity in the passband than do the corresponding filters which have an equiripple amplitude response in the passband. The results obtained show that the increase in sensitivity of the latter filters is not substantial, and so the use of a filter structure which models that of a doubly terminated LC ladder is justified. However, the sensitivity properties of switched-capacitor bandpass and highpass filters require investigation, to determine the effect of the frequency variable terminations on their sensitivity properties. The extension of the sensitivity analysis technique described in Chapter Four to cover switched-capacitor ladder filters of such types would be a simple but useful step.

The low sensitivity properties of switched- capacitor ladder filters justified their use even when an exact design technique was not available. Such filters were then limited to operation at low frequencies, since the approximate design technique used required that the sampling rate greatly exceed the limit imposed by the sampling theorem. Removal of this design constraint has thus allowed switched- capacitor ladder filters to be designed for use at high frequencies [142]. However, special circuitry is required for switched- capacitor filters designed to operate over an extended frequency range.

Circuit topologies have been described which result in reduced settling time requirements for the op-amps in a filter. The benefits of a fully differential filter structure have been outlined. The fully differential filter design of Fig. 5.7 has been proposed for use over an extended frequency range. This requires three op-amps to provide a transfer function with a second-order z-plane numerator, comparable with that of a standard two op-amp biquad, although it features an additional pole. An algorithm for obtaining the capacitor ratios for the proposed filter has been presented. It has been shown that, by means of simple transformations of the circuit, a family of filters similar in structure to that of Fig. 5.7 can be obtained, so that any z-domain transfer function with three poles and two zeros can be implemented. This follows from the versatility of a fully differential filter structure, in which both polarities of filter output are available. Therefore, this family of filters can be used, for example, instead of the family of biquads presented in [23], where high frequency operation is required. A comparative study of the operation of this filter, and of other filter types, numerically evaluating, for example, the effects of finite op-amp bandwidth on the filter response, would be of considerable interest.

Circuitry has been proposed for the implementation of a line equaliser for baseband digital communications. The kernel of the design is a programmable equaliser section based on the circuit of Fig. 5.7, but using programmable capacitor arrays. The pre-filter employed features a third-order continuous-time anti-aliasing filter and a 4:1 sampling rate reduction incorporated in a second order switched-capacitor lowpass ladder filter, with two stages of stray-insensitive cosine filtering. This is implemented economically by exploiting the versatility of a fully differential filter structure.

Techniques for optimising the equaliser section transfer function so as to

minimise the intersymbol interference when the equaliser input is the pulse response of a telephone line have been investigated for various line lengths.

A time domain method which seeks to directly minimise the value of intersymbol interference by optimising the locations of the poles and zeros of the equaliser section has been presented. The results obtained show that this technique results in excellent values for intersymbol interference. A disadvantage of this method is that it offers no control over the frequency response in the system, and, in particular, does not limit the system bandwidth. Pole and zero locations which result in low capacitance ratio spread in the equaliser section, whilst keeping the value of intersymbol interference low, do not result in a finite system bandwidth. Thus, in practice, a very tight specification on the pre-filter, or an additional roll-off filter, which limits bandwidth without substantially increasing intersymbol interference, would be required.

A frequency domain technique has also been investigated. This seeks to optimise the equaliser section response so that the pulse response of the complete system approximates to a cosine roll-off function, which is known to result in zero intersymbol interference [180]. The results obtained indicate that the complexity of the equaliser section is not sufficient to allow a cosine roll-off response to be approximated accurately. The technique results in values for intersymbol interference which are inferior to those for the time domain method, although high frequency attenuation is introduced, at the expense of an increase in capacitor ratio spread.

The results obtained suggest that a hybrid optimisation technique may prove to be superior to both the above methods, wherein the equaliser section transfer function is optimised so as to minimise the intersymbol interference for the equaliser *system*, whilst also minimising the high frequency response of the equaliser *section*.

A technique has been proposed for introducing adaptive operation of the line equaliser. This technique uses a bandpass filter to determine the high frequency attenuation introduced by the line. For this method to be successful, it is critical that the equaliser frequency response should be similar for each of its possible settings, when connected to a line of the length for which the equaliser section transfer function at that setting has been optimised, so that there will be a

correlation between the bandpass filter output and the equaliser misalignment. This requires the use of a frequency domain optimisation algorithm, modified so that the output of the bandpass filter is always above a chosen reference level for over-equalisation, and below it for under-equalisation. Such an optimisation is expected to be very costly in computer time.

Details of a number of the circuits which have been designed have been given to the National Micro-electronics Research Centre (N.M.R.C.) in Cork. These circuits are being fabricated on the 5 μm CMOS process available there. Thus the practical features and limitations of the circuits designed can be assessed. At the time of writing, no information is available about the properties of the integrated filters. A comparison of the actual operation of these filters, the results expected of an ideal filter, and the results from a simulation of the circuits which assigns realistic values to such non-ideal factors as the finite op-amp bandwidth, and switch on-resistances, would be of considerable benefit when designing further switched- capacitor filters for the same target process.

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APPENDIX A: ANALYSIS OF FULLY DIFFERENTIAL INTEGRATORS

A.1: Introduction.

The fully differential counterparts of the *lossless discrete integrator* (l.d.i.) and *damped discrete integrator* (d.d.i.) circuits of [9] will here be analysed. Note that the abbreviated notation

$$f(n) \equiv f(nT)$$

is used to represent a function of time f(t) evaluated at t = nT.

A.2: The Non-inverting L.D.I.

Fig. A-1a shows the structure of a conventional (single-ended) non-inverting l.d.i. Fig. A-1b shows the corresponding circuit for a fully-differential (double-ended) integrator.

Let the two phases of the clock waveform be φ_1 (the odd phase, nominal time of occurrence being from time t = (n-1)T to t = (n-½)T. where n is an integer and T is the clock period) which is the phase illustrated, and φ_2 (the even phase ,occurring from time t = (n-½)T to t = nT). It is assumed that the switches are ideal and that the op-amp can be modelled by the circuit in Fig. A-2.

Consider the odd phase. The circuit on this phase is as shown in Fig. A-3. Let Q_1,Q_2,Q_3,Q_4 be the charges on $C_{1a},C_{1b},C_{2a},C_{2b}$ respectively, where the '+' signs at the capacitors in Fig. A-3 indicate which plate is regarded as having a positive charge.

The input voltages V_1 and V_2 are sampled by C_{1a} and C_{1b}. Thus :

$$Q_1(n-\tfrac{1}{2}) = C_1V_1(n-\tfrac{1}{2}) \qquad (A.1)$$
$$Q_2(n-\tfrac{1}{2}) = C_1V_2(n-\tfrac{1}{2})$$

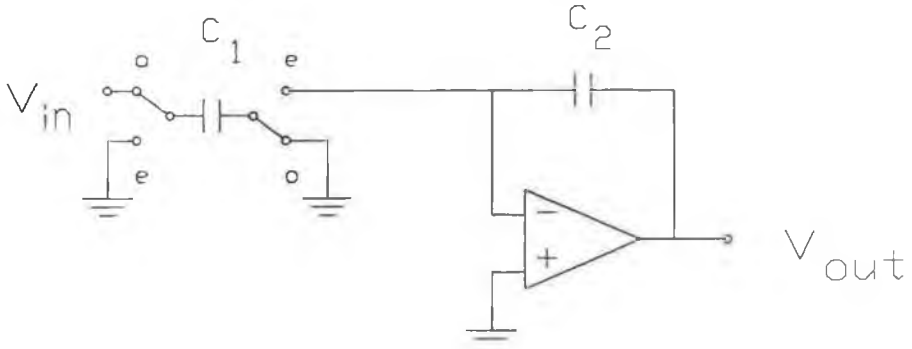


Fig. A-1(a): single-ended non-inverting l.d.i

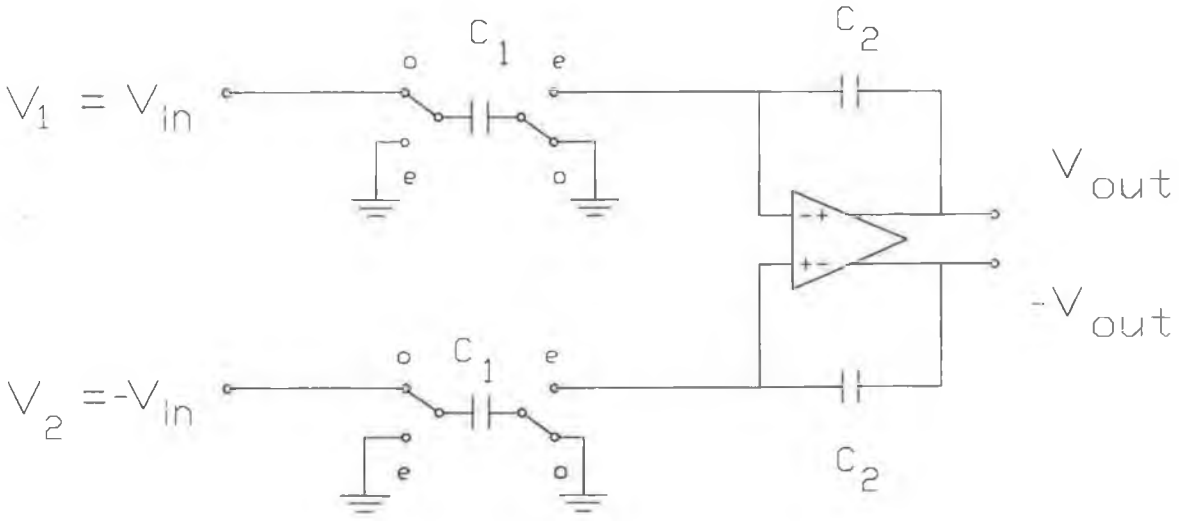


Fig. A-1(b): Double-ended non-inverting l.d.i.

At the start of φ_1, the charges on capacitors C_{2a} and C_{2b} are determined by the voltage differences across them at the end of φ_2.

$$Q_3(n-1) = C_2 \left(V_o(n-1) - V_a(n-1) \right) \qquad (A.2)$$
$$Q_4(n-1) = C_2 \left(-V_o(n-1) - V_b(n-1) \right)$$

The question now arises as to whether the output voltage V_o can change during φ_1, i.e. in the time interval $(n-1)T < t < (n-\frac{1}{2})T$. First note that, on the odd phase, one plate of both C_{2a} and C_{2b} is open-circuited. Thus the charges on these capacitors cannot change during φ_1 .

$$Q_3(n-\tfrac{1}{2}) = Q_3(n-1) \qquad (A.3)$$
$$Q_4(n-\tfrac{1}{2}) = Q_4(n-1)$$

The output voltage is given by

$$V_o(t) = k\, V(t) \qquad , V = V_b - V_a \qquad (A.4)$$

Because Q_3, Q_4 remain constant during φ_1, it follows that the associated voltages remain constant.

$$k\, V(t) - V_a(t) = V_{c_1}, \qquad (A.5)$$
$$(n-1)T < t < (n-\tfrac{1}{2})T$$
$$-k\, V(t) - V_b(t) = V_{c_2},$$
$$V_{c_1}, V_{c_2} \text{ constant values}$$

Thus

$$2k\, V(t) + V_b(t) - V_a(t) = V_{c_1} - V_{c_2} \qquad (A.6)$$

or

$$(2k + 1)\, V(t) = V_{c_1} - V_{c_2}\,, \qquad (A.7)$$
$$(n-1)T < t < (n-\tfrac{1}{2})T$$

Hence, since $k \neq -\frac{1}{2}$ $(k > 0)$ it follows that $V(t)$ and consequently $V_o(t)$ is constant during φ_1 .

$$V_o(n-\tfrac{1}{2}) = V_o(n-1) \qquad (A.8)$$

Now consider the even phase shown in Fig. A-4a which is redrawn in Fig. A-4b for clarity. The output of this circuit, given initial charges on the capacitors, can readily be determined using charge conservation, and will be in the form of a step change from the previous value of output to the new value. However, the case will instead be considered where the voltage sources include source resistance, and the resulting circuit will be analysed in the limit as the resistance becomes negligible. To this end, the circuit of Fig. A-5 will be considered.

The expression for V(t) must be found for this circuit, given that, at time $t = 0^-$, C_1, C_2 are precharged to $Q_1(0^-) = -C_1V_1(0^-)$, $Q_2(0^-) = C_2V_2(0^-)$, and that the voltage source is instantaneously connected into the circuit at time $t = 0$.

Clearly, the current flowing in the circuit is

$$\begin{aligned} i &= [\, V - (V_1+V_2) \,] \,/\, R \\ &= C_2 \, d/dt(V_2) \\ &= C_1 \, d/dt(V_1) \end{aligned} \tag{A.9}$$

Now eliminate V_2 using

$$d/dt(V_2) = (C_1/C_2) \; d/dt(V_1) \tag{A.10}$$

Hence

$$\int_0^t dV_2 = \frac{C_1}{C_2} \int_0^t dV_1 \tag{A.11}$$

So

$$V_2(t) - V_1(t) = (C_1/C_2)(V_1(t) - V_1(0)) \tag{A.12}$$

or

$$V_2(t) = (C_1/C_2)(V_1(t) - V_1(0)) + V_2(0) \tag{A.13}$$

Thus

$$V_1(t) + V_2(t) = [\ (C_1 + C_2)V_1(t) - C_1V_1(0) + C_2(0)\ ]/C_2 \tag{A.14}$$

Hence (A.12) becomes

$$RC_1\,{}^{d}/_{dt}(V_1) = V(t) - V_2(0) - [\ (C_1 + C_2)V_1(t) - C_1V_1(0)\ ]/C_2 \tag{A.15}$$

In the limit as $R \to 0$, the left hand side of (A.15) becomes zero, and we obtain :

Case 1) for $t = 0^+$:

The right hand side of (A.15) is finite unless $V(0) = V_1(0^-) + V_2(0^-)$ so if $R \to 0$ then ${}^{d}/_{dt}(V_1) \to \infty$, i.e. for $R = 0$ there is a step change in $V_1 + V_2$ at time $t = 0$. Clearly in the situation where $V(0) = V_1(0^-) + V_2(0^-)$ no current flows and hence V_1, V_2 are unchanged.

Case 2) for $t > 0$:

After the transient at $t = 0$, the circuit will tend to a steady state and thus the right hand side of (A.15) will become zero. So

$$(C_1 + C_2)/C_2\ V_1(t) = V(t) - V_2(0) + C_1/C_2\ V_1(0) \tag{A.16}$$

or equivalently

$$V_1(t) = [\ C_2V(t) - Q_1(0) - Q_2(0)\ ]/[\ C_1 + C_2\ ] \tag{A.17}$$

It is interesting to note that, for t sufficiently large, this equation is always valid, regardless of the value of R.

Relating the above result to the circuit of Fig. A-4, it follows that

$$V_a(t) = [\ C_2kV(t) - Q_1(n-\tfrac{1}{2}) - Q_3(n-\tfrac{1}{2})]/[C_1 + C_2], \tag{A.18}$$
$$V_b(t) = [-C_2kV(t) - Q_2(n-\tfrac{1}{2}) - Q_4(n-\tfrac{1}{2})]/[C_1 + C_2],$$
$$(n-\tfrac{1}{2})T < t < nT$$

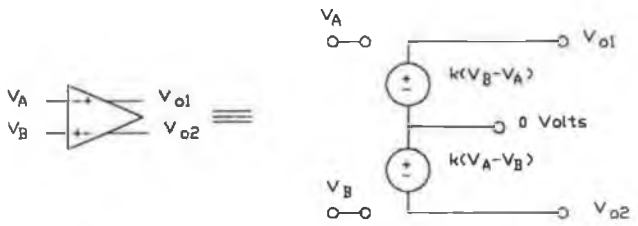


Fig. A-2: Equivalent circuit for fully differential op-amp.

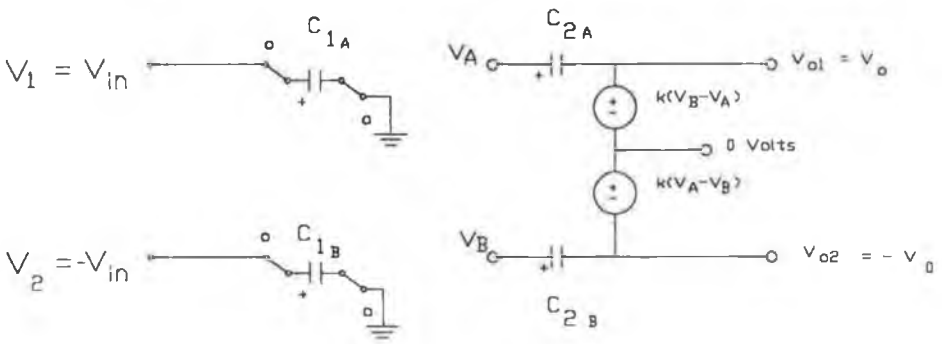
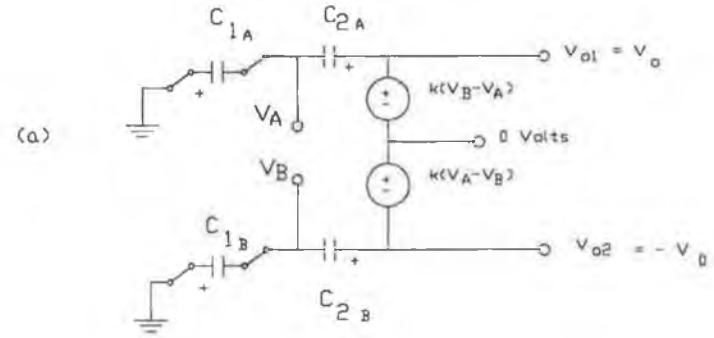


Fig. A-3: non-inverting l.d.i. during odd phase



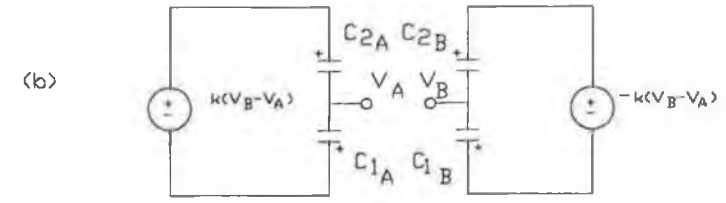


Fig. A-4: non-inverting l.d.i. during even phase.

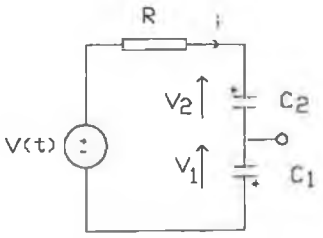


Fig. A-5: see text.

where the initial values of Q_1,Q_2,Q_3,Q_4 are the charges present at the end of φ_1. Therefore

$$V(t) = V_b(t) - V_a(t) \tag{A.19}$$

$$= \frac{-2C_2kV(t) + Q_1(n-\frac{1}{2}) - Q_2(n-\frac{1}{2}) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{C_1 + C_2}$$

and so

$$V(t) = \frac{Q_1(n-\frac{1}{2}) - Q_2(n-\frac{1}{2}) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{C_1 + C_2 + 2kC_2} \tag{A.20}$$

$V_O = k\ V$ so (A.20) to is re-arranged to obtain

$$V_O(t) = \frac{Q_1(n-\frac{1}{2}) - Q_2(n-\frac{1}{2}) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{(C_1 + C_2)/k + 2C_2} \tag{A.21}$$

In the limit as $k \to \infty$ this becomes

$$V_O(t) = \frac{Q_1(n-\frac{1}{2}) - Q_2(n-\frac{1}{2}) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{2C_2} \tag{A.22}$$

Substituting from (A.1), (A.2) and (A.3) for the values of charge at the start of φ_2 yields the following expression for V_O at the end of φ_2 :

$$\begin{aligned} V_O(n) &= (C_1/2C_2) (V_1(n-\tfrac{1}{2}) - V_2(n-\tfrac{1}{2})) \\ &+ 1/2 (V_O(n-1) - V_a(n-1)) \\ &- 1/2 (-V_O(n-1) - V_b(n-1)) \end{aligned} \tag{A.23}$$

or

$$\begin{aligned} V_O(n) &= (C_1/2C_2) (V_1(n-\tfrac{1}{2}) - V_2(n-\tfrac{1}{2})) \\ &+ 1/2 (2V_O(n-1) + V(n-1)) \end{aligned} \tag{A.24}$$

As $k \rightarrow \infty$, $V(n-1) \rightarrow 0$ (from (A.20)), and so, substituting $V_1 = V_{in}$ and $V_2 = -V_{in}$, the following result is obtained :

$$V_o(n) = (C_1/C_2)\, V_{in}(n-\tfrac{1}{2}) + V_o(n-1) \qquad \text{(A.25)}$$

This is the same difference equation as for the single-ended case, under the assumption that all circuit elements are ideal.

A.3: The Non-inverting D.D.I.

The fully differential non-inverting d.d.i. is shown in Fig. A-6. The derivation of the difference equation for this integrator is similar in form to that for the l.d.i. The difference is that, in Fig. A-4, C_2 must be replaced by $C_2 + C_3$, since, on the even phase of the d.d.i. C_{3a} (C_{3b}) is in parallel with C_{2a} (C_{2b}).

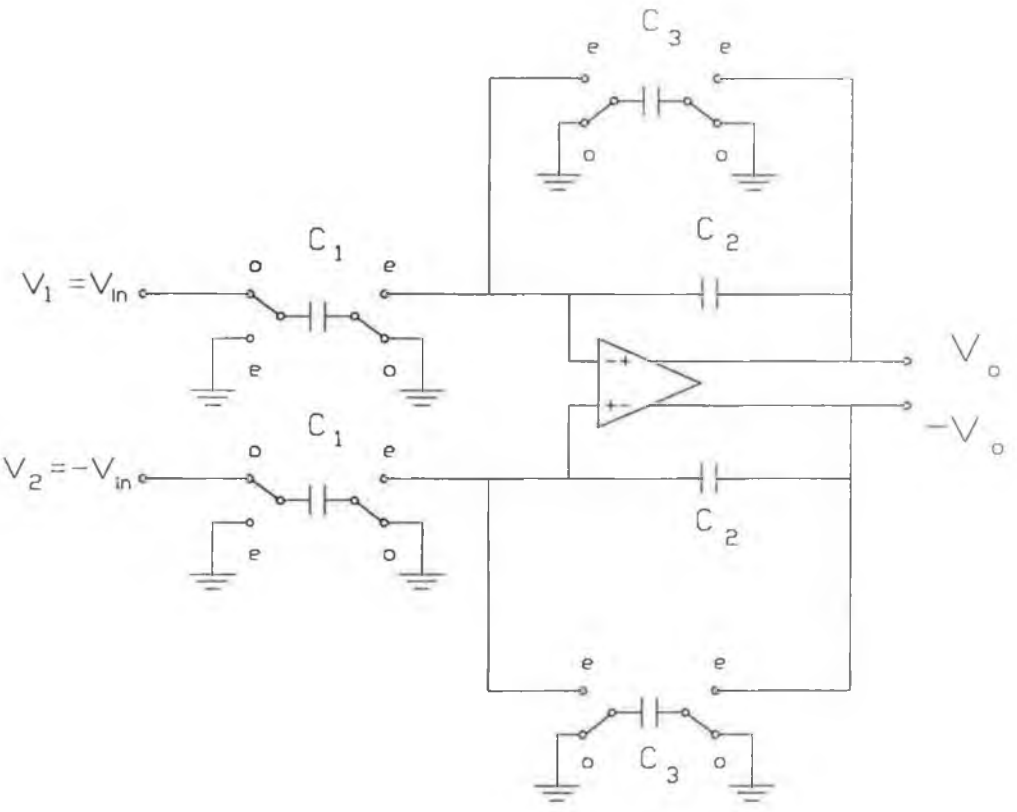


Fig. A-6: Double-ended non-inverting d.d.i.

The damping capacitors C_3 do not contribute any additional charge on φ_2, since they are discharged on φ_1. Thus, for the d.d.i. case, (A.22) becomes :

$$V_0(t) = \frac{Q_1(n-\frac{1}{2}) - Q_2(n-\frac{1}{2}) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{2(C_2 + C_3)} \qquad \text{(A.26)}$$

However, the charges Q_1, Q_2, Q_3, Q_4 at the end of the odd phase are the same as in the l.d.i. case. Thus

$$V_0(n) = (C_1/2(C_2 + C_3)) (V_1(n-\tfrac{1}{2}) - V_2(n-\tfrac{1}{2})) + (C_2/2(C_2 + C_3)) (2V_0(n-1) + V(n-1)) \qquad \text{(A.27)}$$

As in the case of the l.d.i., $V(n-1) \rightarrow 0$, and so, with $V_1 = -V_2 = V_{in}$, the expression for V_0 becomes :

$$V_0(n) = C_1/(C_2 + C_3)\ V_{in}(n-\tfrac{1}{2}) + C_2/(C_2 + C_3)\ V_0(n-1) \qquad \text{(A.28)}$$

This difference equation is again identical to that for the single-ended case.

A.4: The Inverting L.D.I.

Fig. A-7 shows a fully differential inverting l.d.i. During the odd phase, the circuit is identical to Fig. A-3, with the exception that both terminals of C_{1a} and C_{1b} are connected to earth, so

$$V_0(n-\tfrac{1}{2}) = V_0(n-1) \qquad \text{(A.29)}$$
$$Q_1(n-\tfrac{1}{2}) = Q_2(n-\tfrac{1}{2}) = 0$$

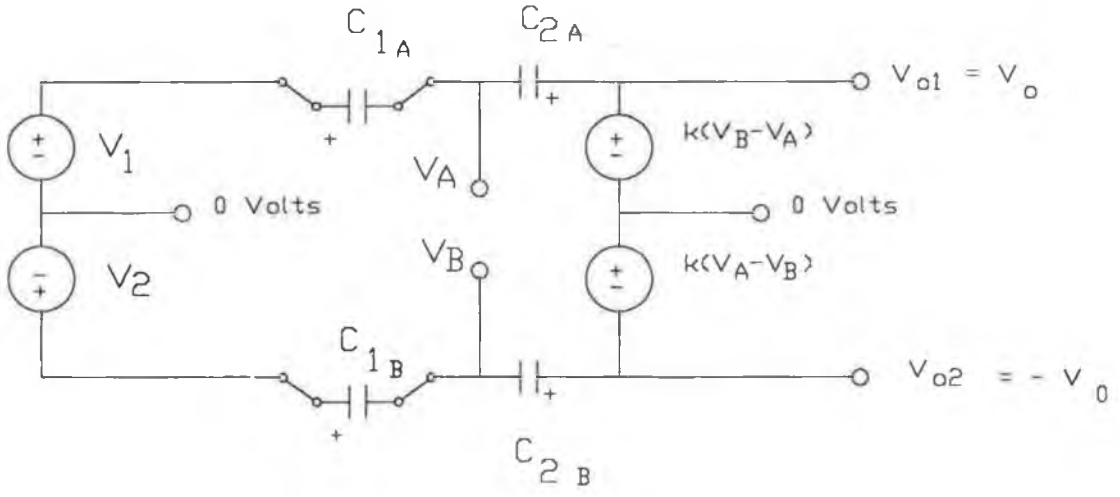


Fig. A-8: inverting l.d.i. - even phase.

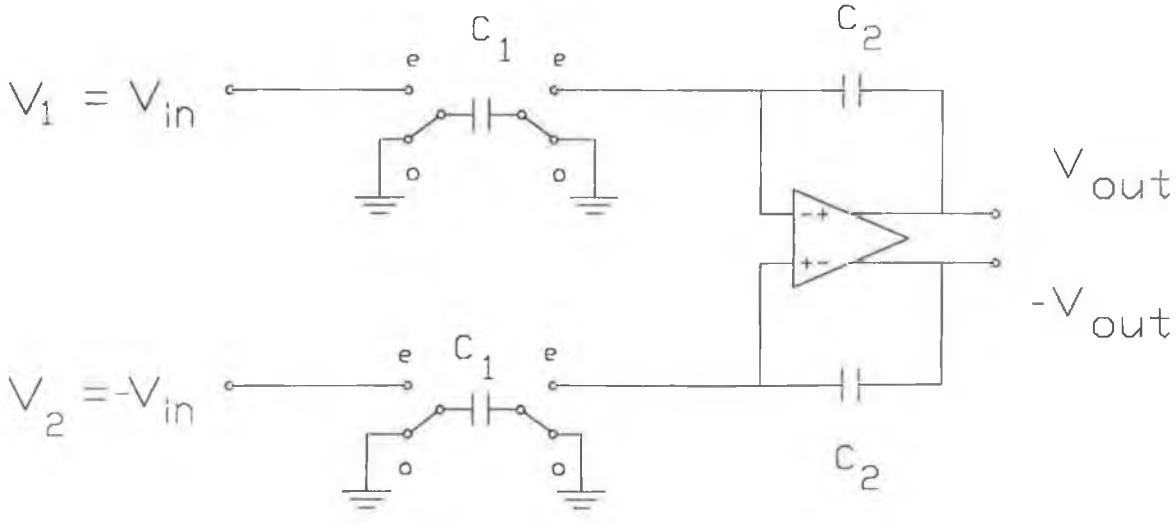


Fig. A-7: Double-ended inverting l.d.i.

During the even phase, the circuit is as shown in Fig. A-8. By a simple extension to the equations for Fig. A-4 to account for the presence of V_1 and V_2, (A-18) becomes

$$V_a(t) = V_1(t) + \frac{C_2(kV(t) - V_1(t)) - Q_3(n-\frac{1}{2})}{C_1 + C_2,} \qquad (A.30)$$

$$V_b(t) = V_2(t) + \frac{C_2(-kV(t) - V_2(t)) - Q_4(n-\frac{1}{2})}{C_1 + C_2,}$$

$$(n-\tfrac{1}{2})T < t < nT$$

Thus

$$V(t) = V_b(t) - V_a(t) \qquad (A.31)$$

$$= V_2(t) - V_1(t)$$

$$+ \frac{- 2C_2kV(t) - C_2V_2(t) + C_2V_1(t)) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{C_1 + C_2}$$

and so

$$V(t) = \frac{C_1V_2(t) - C_1V_1(t) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{C_1 + C_2 + 2kC_2} \qquad (A.32)$$

Hence (A.32) to is re-arranged to obtain

$$V_O(t) = \frac{C_1V_2(t) - C_1V_1(t) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{(C_1 + C_2)/k + 2C_2} \qquad (A.33)$$

Substituting from (A.2) and (A.3) for the values of charge at the start of φ_2 and in the limit as $k \to \infty$ yields the following expression for V_O at the end of φ_2:

$$V_o(n) = (C_1/2C_2) (V_2(n) - V_1(n)) + 1/2 (V_o(n-1) - V_a(n-1)) - 1/2 (-V_o(n-1) - V_b(n-1)) \quad (A.34)$$

or

$$V_o(n) = (C_1/2C_2) (V_2(n) - V_1(n)) + 1/2 (2V_o(n-1) + V(n-1)) \quad (A.35)$$

As $k \to \infty$, $V(n-1) \to 0$ (from (A.32)), and so, substituting $V_1 = V_{in}$ and $V_2 = -V_{in}$, the following result is obtained :

$$V_o(n) = - (C_1/C_2) V_{in}(n) + V_o(n-1) \quad (A.36)$$

This is the same difference equation as for the single-ended inverted integrator, under the assumption that all circuit elements are ideal.

A.5: The Inverting D.D.I.

The above derivation of the difference equation describing the inverting l.d.i. can readily be extended to the case of the inverting d.d.i. shown in Fig. A-9. The details of the derivation will not be given here, as it is largely a repetition of the equations above. As with the non-inverting d.d.i., C_2 is replaced by $C_2 + C_3$ in the appropriate equations, e.g. (A.32), (A.33). Thus (A.33) becomes

$$V_o(t) = \frac{C_1V_2(t) - C_1V_1(t) + Q_3(n-\frac{1}{2}) - Q_4(n-\frac{1}{2})}{(C_1 + C_2 + C_3)/k + 2(C_2 + C_3)} \quad (A.37)$$

Substituting from (A.2) and (A.3) for the values of charge at the start of φ_2 and in the limit as $k \to \infty$ yields the following expression for V_o at the end of φ_2:

$$V_o(n) = C_1/2(C_2 + C_3) (V_2(n) - V_1(n)) + C_2/2(C_2 + C_3) (V_o(n-1) - V_a(n-1)) - C_2/2(C_2 + C_3) (-V_o(n-1) - V_b(n-1)) \quad (A.38)$$

or

$$V_O(n) = C_1/2(C_2 + C_3)\ (\ V_2(n) - V_1(n)\ )$$
$$+\ C_1/2(C_2 + C_3)\ (2V_O(n-1) + V(n-1)\ ) \qquad \text{(A.39)}$$

As $k \to \infty$, $V(n-1) \to 0$, and so, substituting $V_1 = V_{in}$ and $V_2 = -V_{in}$, the expected result, identical to that for the single-ended case, is obtained :

$$V_O(n) = -\ C_1/(C_2 + C_3)\ V_{in}(n)$$
$$+\ C_2/(C_2 + C_3)\ V_O(n-1) \qquad \text{(A.40)}$$

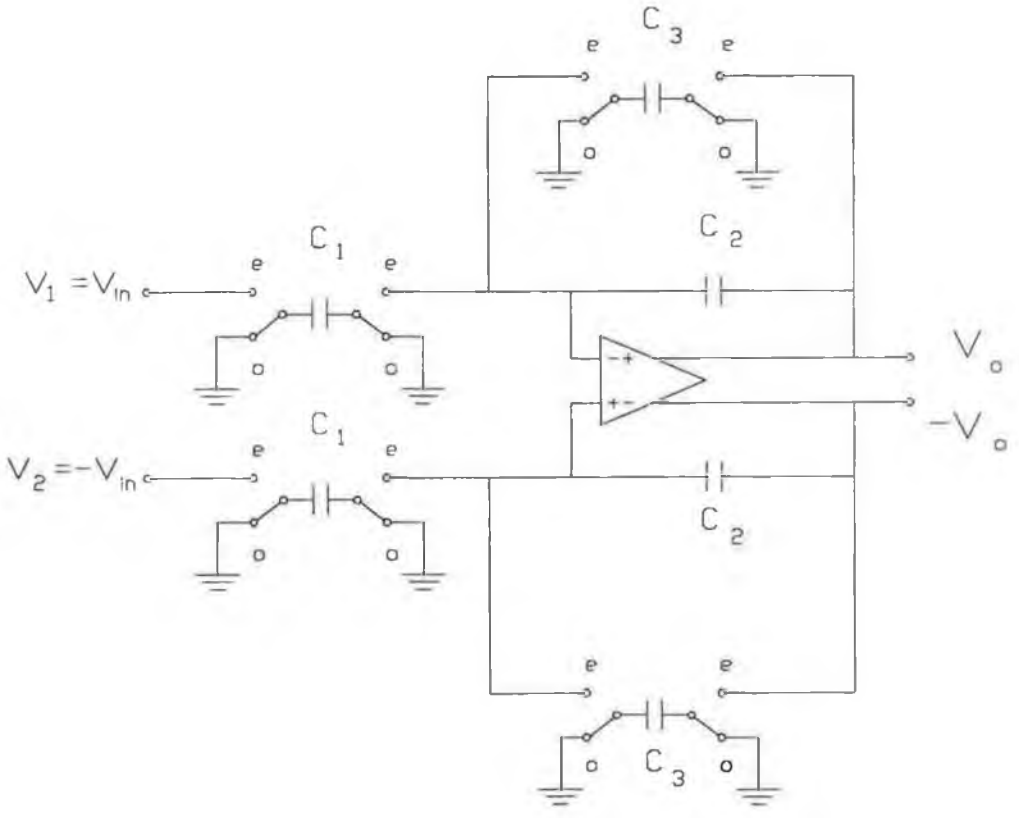


Fig. A-9: Double-ended inverting d.d.i.

A.6: The Differencing-input Integrator.

Because both polarities of the filter output are available in double-ended switched-capacitor filters, additional circuit topologies are possible which would require additional inverting circuits with single-ended designs. One example is the integrator shown in Fig. A-10, which is known as a *differencing-input integrator*.

This consists of a d.d.i. which provides non-inverting integration for V_1, and inverting integration for V_2. It can readily be shown (e.g. by a straight-forward application of superposition using equations (A.28) and (A.40)) that the circuit output is

$$V_0(n) = \frac{C_2V_0(n-1) - C_1V_2(n) + C_1V_1(n-\frac{1}{2})}{C_2 + C_3} \qquad (A.41)$$

If we choose $V_1 = -V_2 = V_{in}$ then

$$V_0(n) = \frac{C_2V_0(n-1) + C_1\,(\,V_1(n) + V_1(n-\frac{1}{2})\,)}{C_2 + C_3} \qquad (A.42)$$

The same operation can be obtained with a reduced number of capacitors using the circuit of Fig. A-11.

The exact form of the transfer function implemented by a switched-capacitor integrator which nominally implements the l.d.i. or d.d.i. depends on when the input samples are held, and is particularly important for differencing- input integrators :

Case 1) V_{in} is held during the even phase, i.e.

$$V_{in}(n) = V_{in}(n-\tfrac{1}{2}) \qquad (A.43)$$

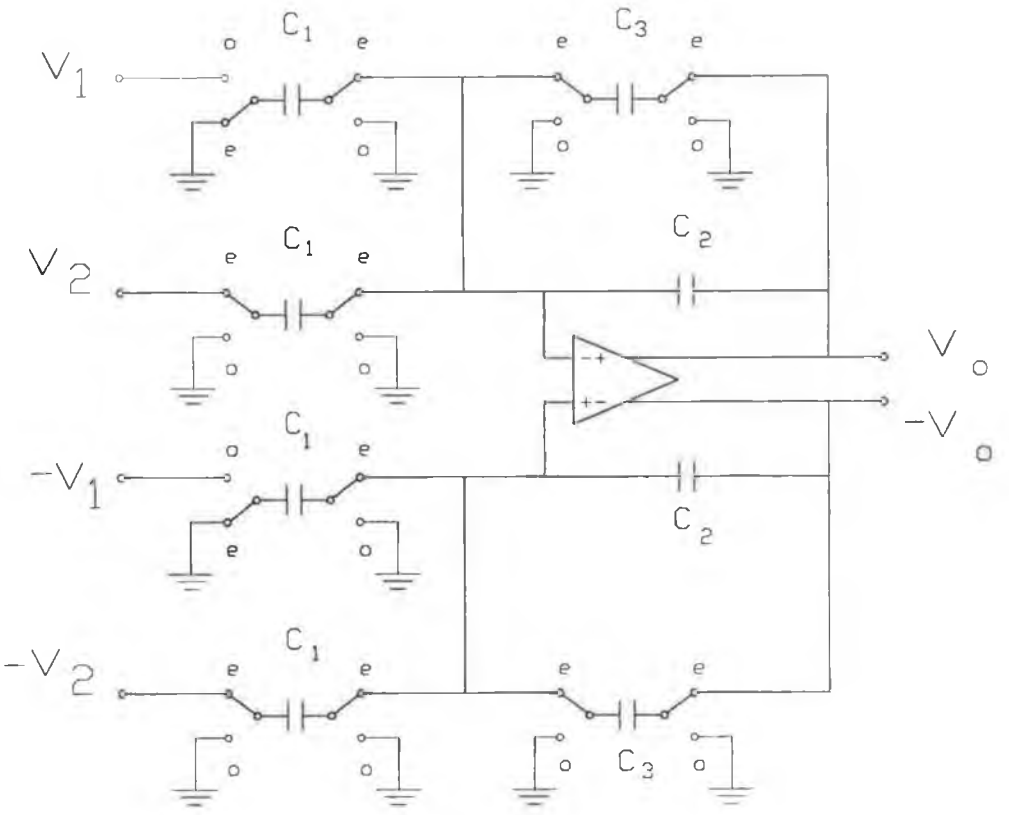


Fig. A-10: Differencing input integrator.

Then

$$V_o(n) = \frac{C_2 V_o(n-1) + 2C_1 V_{in}(n-\frac{1}{2})}{C_2 + C_3} \qquad (A.44)$$

This is the difference equation of a standard non-inverting d.d.i. with the exception that C_1 in this case need only be half the value for a standard d.d.i.

Case 2) V_{in} is held during the odd phase, i.e.

$$V_{in}(n-\tfrac{1}{2}) = V_{in}(n-1) \qquad (A.45)$$

Then

$$V_o(n) = \frac{C_2 V_o(n-1) + C_1 \left(V_{in}(n) + V_{in}(n-1) \right)}{C_2 + C_3} \qquad (A.46)$$

This equation corresponds to a damped integrator of the bilinear type , i.e. based on the use of the variable

$$\lambda = \frac{1 - z^{-1}}{1 - z^{-1}}$$

to obtain a discrete-time approximation of integration.

Therefore, this approach allows the exact implementation of a filter which simulates a passive prototype, using the bilinear transformation. However, such an approach, which leads to delay-free loops in digital filters [10,168], will, in switched-capacitor filters, lead to a structure where, on one of the clock phases, there will be a path for charge connecting all filter stages. Since this will mean that the filter will have a long settling time on this phase, such a structure is not suitable for high frequency operation.

Case 3) V_{in} changes from phase to phase

This can occur if V_{in} is the output of a sampled-data filter operating at twice the sampling rate of the differencing-input integrator, or if it is a continuous-time waveform. In this case, we can write

$$V_o(n) = \frac{C_2 V_o(n-1) + 2C_1 V'_{in}(n)}{C_2 + C_3} \qquad (A.47)$$

where

$$V'_{in}(n) = \tfrac{1}{2} \left(V_{in}(n) + V_{in}(n-\tfrac{1}{2}) \right) \qquad (A.48)$$

(A.47) is the equation of a non-inverting d.d.i. with the exception that the usual delay of $T/2$ through the integrator is not present. (A.48) is the equation of a cosine filter [175] which is used to filter out potentially aliased frequency components before decimation. Therefore, in this case, the differencing-input integrator is suitable for use as a filter input stage.

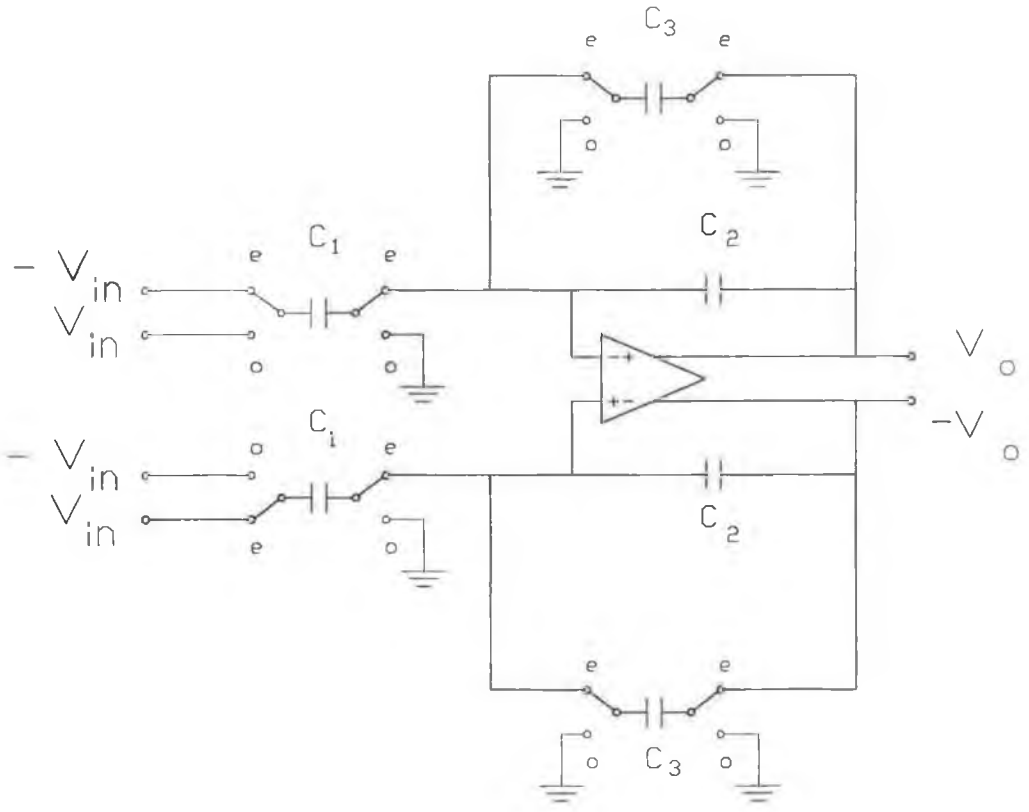


Fig. A-11: Differencing-input integrator - alternative circuit.

APPENDIX B: ANALYSIS OF PROPOSED FILTER STRUCTURE

A transfer function is derived for the single-ended filter proposed in Chapter 5, the circuit of which is shown in Fig. B-1.

The convention will be adopted of referring to a voltage v(t) as v(n) at the end of φ_2 and as $v(n-\frac{1}{2})$ at the end of φ_1.

The first stage is a standard d.d.i. with its output changing on φ_1. Thus

$$V_1(n+\tfrac{1}{2}) = \frac{C_{21}V_1(n-\tfrac{1}{2}) + C_{1a_1}V_{in}(n) - C_{1b_1}V_2(n+\tfrac{1}{2})}{C_{21} + C_{31}} \qquad (B.1)$$

The second stage is similar, with an output changing on φ_2

$$V_2(n) = \frac{C_{22}V_2(n-1) + C_{12}V_1(n-\tfrac{1}{2})}{C_{22} + C_{32}} \qquad (B.2)$$

The third stage output changes on φ_1.

$$V_3(n+\tfrac{1}{2}) = \frac{C_{23}V_3(n-\tfrac{1}{2}) + C_{1a_3}V_{in}(n) + C_{1b_3}V_1(n) + C_{1c_3}V_2(n)}{C_{23} + C_{33}} \qquad (B.3)$$

Since $V_2(n+\frac{1}{2}) = V_2(n)$ (B.1) becomes

$$V_1(n+\tfrac{1}{2}) = \frac{C_{21}V_1(n-\tfrac{1}{2}) + C_{1a_1}V_{in}(n) - C_{1b_1}V_2(n)}{C_{21} + C_{31}} \qquad (B.4)$$

The z-transforms of (B.2)-(B.4) are :

$$z^{1/2}\, V_1(z) = \frac{k_{a_1} V_{in}(z) - k_{b_1} V_2(z)}{1 - k_{d_1}\, z^{-1}} \tag{B.5}$$

$$V_2(z) = \frac{k_{a_2}\, z^{-1/2}\, V_1(z)}{1 - k_{d_2}\, z^{-1}} \tag{B.6}$$

$$z^{1/2}\, V_3(z) = \frac{k_{a_3} V_{in}(z) + k_{b_3} z^{-1/2} V_1(z) + k_{c_3} V_2(z)}{1 - k_{d_3}\, z^{-1}} \tag{B.7}$$

where

$$\begin{aligned} k_{a_1} &= C_{1a_1} / (C_{21} + C_{31}) \\ k_{a_2} &= C_{12} / (C_{22} + C_{32}) \\ k_{a_3} &= C_{1a_3} / (C_{23} + C_{33}) \\ \\ k_{b_1} &= C_{1b_1} / (C_{21} + C_{31}) \\ k_{b_3} &= C_{1b_3} / (C_{23} + C_{33}) \\ \\ k_{c_3} &= C_{1c_3} / (C_{23} + C_{33}) \\ \\ k_{d_1} &= C_{21} / (C_{21} + C_{31}) \\ k_{d_2} &= C_{22} / (C_{22} + C_{32}) \\ k_{d_3} &= C_{23} / (C_{23} + C_{33}) \end{aligned} \tag{B.8}$$

Expressions for $V_1(z)$ and $V_2(z)$ can now be derived. From (B.5),(B.6)

$$V_2(z) = \frac{k_{a_2} z^{-1} (k_{a_1} V_{in}(z) - k_{b_1} V_2(z))}{(1 - k_{d_2}\, z^{-1}) (1 - k_{d_1}\, z^{-1})} \tag{B.9}$$

so

$$V_2(z) = \frac{z^{-1}\, k_{a_1}\, k_{a_2}\, V_{in}(z)}{N(z)} \tag{B.10}$$

where

$$N(z) = (1 - k_{d_2}\, z^{-1})(1 - k_{d_1}\, z^{-1}) + k_{b_1} z^{-1} \tag{B.11}$$

It follows that

$$z^{1/2} V_1(z) = \frac{k_{a_1}\, N(z)\, V_{in}(z) - k_{b_1} k_{a_1} k_{a_2}\, z^{-1}\, V_{in}(z)}{(1 - k_{d_1}\, z^{-1})\, N(z)} \tag{B.12}$$

$$= \frac{k_{a_1}\, (1 - k_{d_2}\, z^{-1})\, V_{in}(z)}{N(z)} \tag{B.13}$$

V_3 is therefore, from (B.13), (B.10) and (B.7), given by:

$$z^{1/2} V_3(z) = \frac{k_{a_3} N(z) + z^{-1} k_{b_3} k_{a_1} k_{a_2} + k_{a_1} k_{c_3}\, (1 - k_{d_2} z^{-1})}{(1 - k_{d_3}\, z^{-1})\, N(z)} \times V_{in}(z) \tag{B.14}$$

Re-arranging (B.14), and observing that the filter output $V_O(z)$ is equal to $V_3(z)$, the following transfer function for the filter is obtained :

$$\frac{V_O(z)}{V_{in}(z)} = \frac{z^{-0.5}\, (a_0 + a_1 z^{-1} + a_2 z^{-2})}{(1 - b_0 z^{-1})\, (b_1 + b_2 z^{-1} + b_3 z^{-2})} \tag{B.15}$$

where :

$$
\begin{aligned}
a_0 &= ka_3 \ ; \\
a_1 &= -\ ka_3(kd_1+kd_2) + ka_3ka_2kb_1 \\
&\qquad + kb_3ka_1 \ + kc_3ka_1ka_2 \ ; \\
a_2 &= ka_3kd_1kd_2 - kb_3ka_1kd_2 \ ; \\
b_0 &= kd_3 \ ; \\
b_1 &= 1.0 \ ; \\
b_2 &= kb_1ka_2 - kd_1 - kd_2 \ ; \\
b_3 &= kd_1kd_2 \ ;
\end{aligned}
\qquad \text{(B.16)}
$$

and where the k co-efficients are given by (B.8).

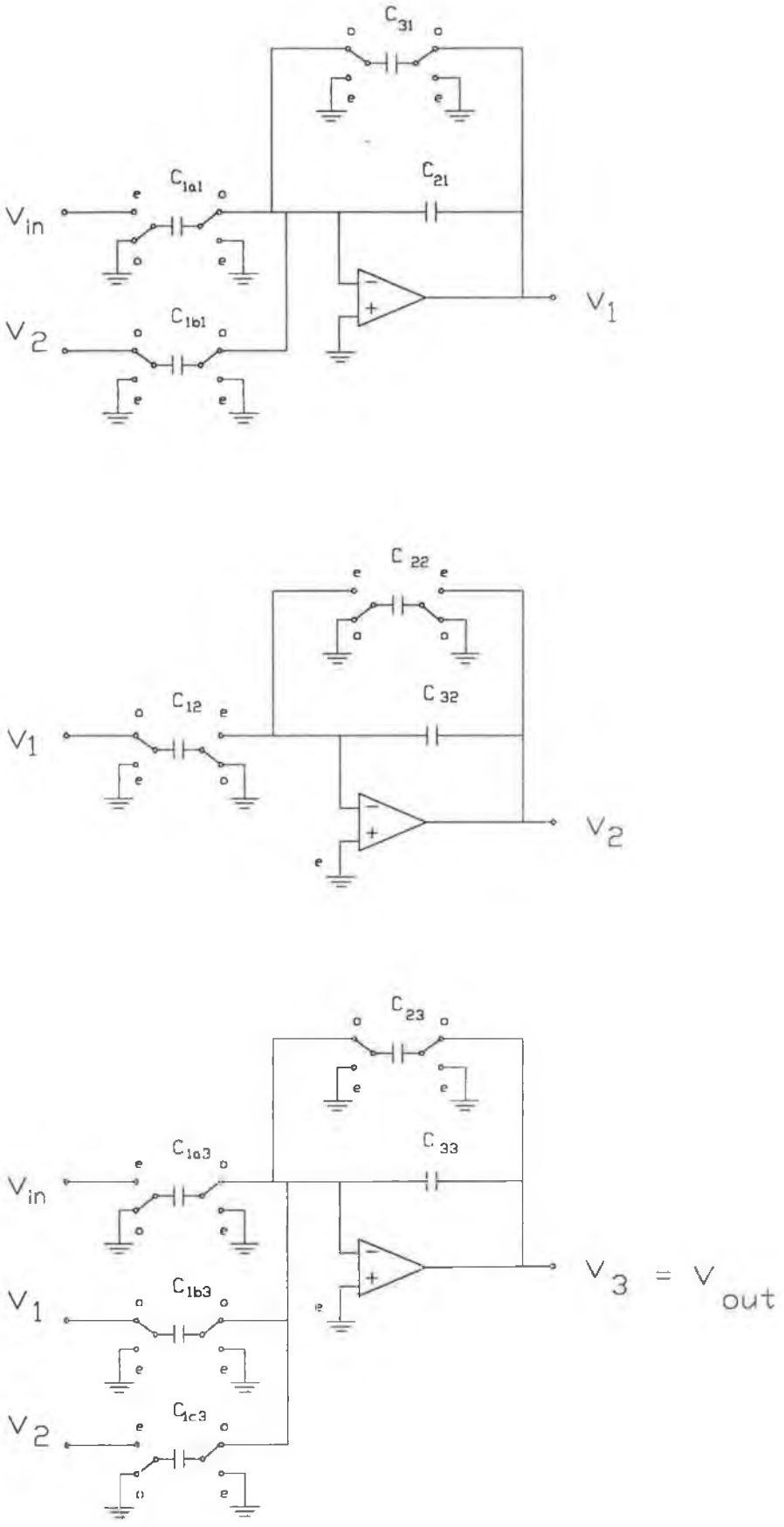


Fig. B-1: Proposed filter, Single-ended Version